RAPID SINGLE FLUX QUANTUM LOGIC
IN HIGH TEMPERATURE SUPERCONDUCTOR TECHNOLOGY

Graduation Committee:

Chairman and Secretary:
Prof. Dr. F. G. Bliek (University of Twente, The Netherlands)

Promotor:
Prof. Dr. H. Rogalla (University of Twente, The Netherlands)

Assistant promotor:
Dr. Ir. A. Brinkman (University of Twente, The Netherlands)

Members:
Prof. Dr. D. Winkler (Chalmers University of Technology, Sweden)
Prof. Dr. Ir. P. van Loosdrecht (University of Groningen, The Netherlands)
Prof. Dr. Ir. H. Zandvliet (University of Twente, The Netherlands)
Prof. Dr. Ing. D. H. A. Blank (University of Twente, The Netherlands)
Dr. Ir. H. G. Kerhoff (University of Twente, The Netherlands)

The work described in this thesis was carried out at the Low Temperature Division of the Faculty of Science and Technology and MESA$^+$ Institute for Nanotechnology of the University of Twente and has been financially supported by the European community through the SuperADC project.

Karthikeyan Shunmugavel,
Rapid Single Flux Quantum Logic in High Temperature Superconductor Technology
Ph.D. Thesis, University of Twente, Enschede, The Netherlands.

ISBN: 90-365-2429-6

Printed by PrintPartners Ipskamp, Enschede.

RAPID SINGLE FLUX QUANTUM LOGIC IN HIGH TEMPERATURE SUPERCONDUCTOR TECHNOLOGY

DISSERTATION

to obtain
the doctor's degree at the University of Twente,
on the authority of the rector magnificus,
prof. dr. W. H. M. Zijm,
on account of the decision of the graduation committee,
to be publicly defended
on Friday 13 October 2006 at 13.15

by

Karthikeyan Shunmugavel
born on 11 May 1976
in Srivilliputtur, India

This dissertation has been approved by the promotor:

Prof. Dr. Horst Rogalla

and the assistant promotor:

Dr. Ir. Alexander Brinkman

தொட்டனைத்து ஊறும் மணற்கேணி மாந்தர்க்குக்
கற்றனைத்து ஊறும் அறிவு.

திருவள்ளுவர்

In sandy soil, when deep you delve, you reach the springs below.
The more you learn, the freer streams of wisdom flow.

Thiruvalluvar from Thirukkural

Translated by Rev. Dr. G. U. Pope

Contents

Chapter 1

Introduction

1.1 Introduction

Superconducting materials lose their electrical resistivity when they are cooled below a certain temperature. It was first discovered in mercury by the Dutch physicist Kamerlingh Onnes in 1911. The temperature below which superconductivity occurs is known as the critical or transition temperature, T_C. Another important property of a superconductor is ideal diamagnetism as discovered by Meissner. When a superconducting material placed in a magnetic field is cooled below its critical temperature, magnetic flux is excluded from the material.

After the discovery of superconductivity, many metals, alloys and compounds were found to be superconductors. In 1957, a successful theory to explain the superconductivity in low T_C materials was developed by L. Bardeen, L. N. Cooper, and J. L. Schrieffer (BCS) [1]. In the superconducting state, two electrons attract each other through the exchange of a virtual phonon and form a Cooper pair. This interaction leads to an energy gap between the BCS ground state and the first excited state in a superconductor. The average distance between the electrons in a Cooper pair is known as the coherence length. A long range interaction exists between the Cooper pairs resulting in a macroscopic quantum state, which can be represented by a common wave function ψ.

Tunneling of Cooper pairs between two superconductors through a barrier was proposed by B. D. Josephson in 1962 [2]. The Josephson junction is the active device used in superconductor electronics. Since then a lot of effort was made to realize Josephson junctions in thin film technology. With the invention of the SQUID (Superconducting Quantum Interference Device), many electronic and microwave devices have been developed based on the Josephson effect.

In 1986, a new ceramic superconductor, Lanthanum barium copper oxide ($LaBa_2Cu_3O_7$) was discovered by Bednorz and Muller with a T_C above 30 K [3]. Soon after this discovery, another ceramic material, Yttrium barium copper oxide ($YBa_2Cu_3O_7$), was found to have a transition temperature above 90 K [4]. In these so-called 123 compounds, superconductivity is thought to exist in the copper oxide planes and it is affected by a change in the oxygen stoichiometry in the layered structure. High quality thin films of these materials can be grown epitaxially on a single crystal substrate at a temperature above 700 ^{0}C by magnetron sputtering and pulsed laser deposition. The superconducting phase is obtained by using post annealing steps in an oxygen environment. Different types of high temperature superconducting (HTS) junction technologies have been explored. Grain boundary junctions [5], ramp type junctions [6] and interface engineered junctions [7] are widely fabricated for different applications.

A new Josephson junction logic called Rapid Single Flux Quantum Logic (RSFQ) was introduced in 1985 by K. K. Likharev, O. A. Mukhanov and V. K. Semenov [8, 9] from Moscow state university. RSFQ deals with the generation and manipulation of magnetic flux quanta in the form of short voltage pulses across a Josephson weak link interrupting a superconducting loop. The fast switching time of Josephson junctions of the order of picoseconds, and the low power dissipation make them suitable for high speed data processing in wire-less technology, military applications, high speed computing and digital signal processing circuits.

Nowadays, high performance superconducting electronic circuits having more than 100,000 junctions are fabricated in low temperature Niobium technology [10]. Despite a lot of challenges in high temperature superconducting technology, simple RSFQ circuits have been demonstrated by various groups [11-14].

1.2 Motivation

With the discovery of high *Tc* materials, the availability of superconducting electronic circuits operating above the liquid Helium temperature came into sight, thereby reducing the refrigeration costs.

In contrast to low T_C junctions, high T_C junctions are intrinsically shunted and exhibit non-hysteretic *IV* characteristics that are suitable for logic operations. Since no shunt resistor is required as in low T_C junctions, this makes the circuit design easier and enhances the circuit density.

In RSFQ circuits, the operating speed is determined by the I_CR product. Josephson junctions should have a non-hysteretic (single-valued) *IV* characteristic to be used in RSFQ circuits. This condition requires a value of the Stewart-McCumber parameter β_C less than unity. It is written as

$$\beta_C = \frac{2\pi R^2 I_C C}{\Phi_0} < 1. \tag{1.1}$$

Φ_0 is the flux quantum and I_C and C are the critical current and capacitance of the Josephson junction respectively. R is the junction resistance, including all in- and extrinsic shunts. By taking β_C as unity, and taking the speed (ν) to be proportional to the product of I_C and R, we arrive at

$$\nu \propto \sqrt{\frac{\Phi_0 I_C}{2\pi C}}. \tag{1.2}$$

Now, the speed depends both on the critical current and the capacitance of the junction. In this respect, it is often said that high T_C junctions are not more beneficial than low T_C junctions [15]. C is indeed solely determined by the junction geometry and the barrier. But the maximum achievable I_C is related to the superconducting energy gap (Δ) of the electrodes via the relation

$$I_C R_N \propto \Delta, \tag{1.3}$$

where the value of the normal state resistance R_N is given by the junction resistance in the absence of any in- or extrinsic shunts. This means that the critical current of a high T_C junction can be increased as compared to a low T_C junction by properly choosing the barrier material because of the larger energy gap. This dependence of I_C on Δ then gives

$$\nu \propto \sqrt{\Delta} \propto \sqrt{T_C} \ . \tag{1.4}$$

The maximum achievable speed ν is thus proportional to the square root of the energy gap, which is higher for high T_C materials.

Despite these advantages of using high T_C materials, realizing a reproducible and controllable junction technology is still a challenge for useful applications. A fully epitaxial layer growth with a clean interface between layers is required for HTS device fabrication. A short coherence length (less than 0.2 nm along the c-axis direction and 1-2 nm along the ab-direction) has lead to the development of various junction geometries to realize the Josephson effect in HTS technology. The order parameter in high T_C materials has a predominantly $d_{x^2-y^2}$ symmetry. Bending of the electronic band structure, faceting at the interface, along with the $d_{x^2-y^2}$ symmetry predict an angle dependent critical current density, related to the orientation of the barrier [16]. Hence, a perfect alignment of the barrier layer with respect to the electrode along the ab-direction is required to reduce the spread in junctions' parameters. Thermally activated switching errors will be dominant at higher temperatures. Careful design is, therefore, necessary to reduce the bit error rate of high T_C circuits.

1.3 Thesis outline

Section 1.4 of this chapter gives an introduction to Josephson phase dynamics. The equivalent circuit of the Josephson junction will be explained to understand the dynamics of the junction under different damping conditions.

Chapter 2 describes the fabrication of ramp type HTS junctions using Neodymium Barium Copper Oxide (NBCO) as superconducting electrodes. Requirements of realizing multilayer ramp type junctions in HTS technology, fabrication and measurements of NBCO junctions and SQUIDs are described.

Chapter 3 focuses on the design of RSFQ circuits. The basic RSFQ components, as well as design issues and the mask-layout processes are described.

Chapter 4 deals with oversampling delta-sigma modulators. Oversampling at GHz rates and the quantum-mechanically accurate feedback using Josephson junctions lead to the development of Delta-Sigma modulators in superconducting electronics with a high dynamic range. A superconducting second order Delta-Sigma modulator is designed and simulated. The possibility to realize a complex modulator circuit in HTS technology is discussed.

Chapter 5 describes the design and optimization of pulse stretcher circuits (SFQ/DC converter with set and reset inputs), fabrication and a successful operation of the circuit experimentally in HTS technology.

Chapter 6 discusses possible ways of connecting the pulse stretcher to other RSFQ circuits for interfacing with room temperature electronics.

1.4 Josephson phase dynamics

1.4.1 Magnetic flux quantization

Superconductivity is a macroscopic quantum phenomenon. All the Cooper pairs form a macroscopic quantum state, which is described by a single wave function

$$\psi = |\psi| e^{i\theta}, \tag{1.5}$$

where $|\psi|^2 = n_s$ is the volume density of the cooper pair and θ is the phase of the wave function.

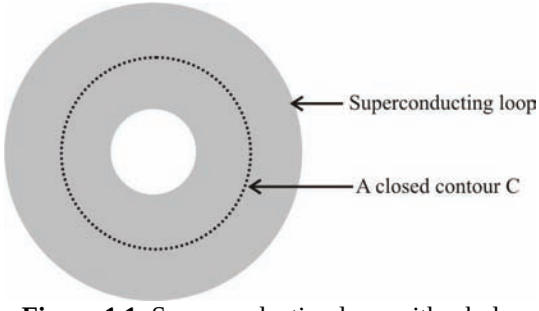


Figure 1.1: Superconducting loop with a hole.

The supercurrent density J_S in a superconductor is given by the following equation.

$$\vec{J}_S = -\frac{n_s e^2}{m}\left(\vec{A} - \frac{h}{4\pi e}\Delta\theta\right), \tag{1.6}$$

where m is the effective mass of the cooper pair, $\vec{A}$ is the magnetic vector potential, e is the electronic charge. Integrating equation (1.6) around a closed contour C (figure 1.1) gives

$$\int_C \left(\frac{m}{n_s e^2}\right)\vec{J}_S.d\vec{l} + \int_S \vec{B}.\vec{ds} = n\Phi_0 \text{ , n=0, 1, 2,……,} \tag{1.7}$$

where Φ_0 is the flux quantum given by

$$\Phi_0 = \frac{h}{2e} = 2.07\times10^{-15} Wb. \tag{1.8}$$

Equation (1.7) is known as the fluxoid quantization equation. If the superconducting loop has a thickness larger than the London penetration depth, and when the contour is taken deeper inside the loop so that J_S is zero, equation (1.8) becomes,

$$\int_S \vec{B}.\vec{ds} = n\Phi_0. \tag{1.9}$$

The magnetic flux trapped in a superconducting loop is quantized in units of the flux quantum.

1.4.2 The Josephson junction

Two superconductors, S_1 and S_2 separated by a thin insulating layer (figure 1.1a), form a Josephson junction. Tunneling of supercurrent in the form of Cooper pairs across the barrier without applying any voltage was predicted by Josephson in 1962. The magnitude of the supercurrent is given by

$$I_S = I_C \sin(\theta_1 - \theta_2), \tag{1.10}$$

where I_C is the maximum value of the supercurrent, which can flow through the junction without developing any voltage (figure 1.1b). $\theta_1 - \theta_2$ is the phase difference between the wave functions in the two superconductors. Relation (1.11) is known as the dc Josephson effect.

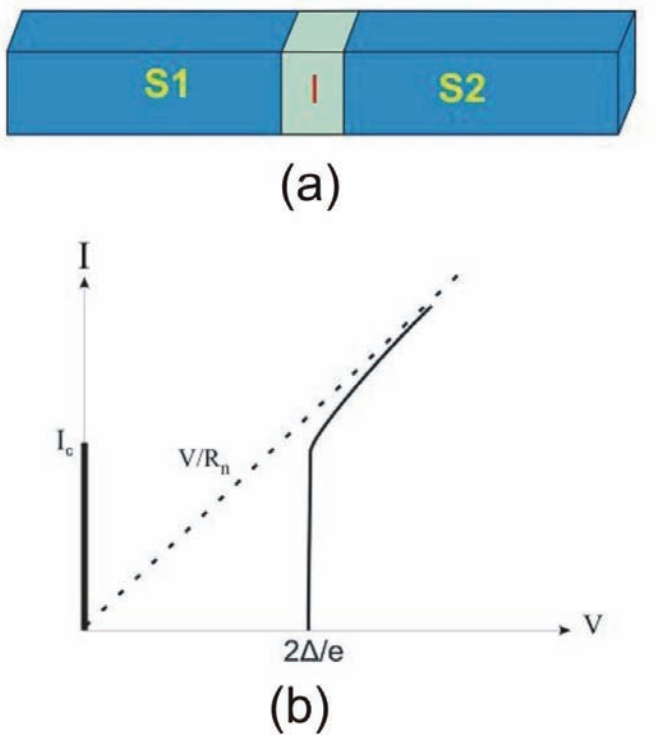


Figure 1.2: a) Josephson junction as a weak link between two superconductors, b) IV curve for a classical junction at T=0.

The magnitude of the critical current, which can be derived from the microscopic theory [17], is given by

$$I_C = \frac{\pi\Delta}{2eR_N} \text{ for } T \ll T_C, \tag{1.11}$$

where Δ is the superconducting energy gap and R_N is the normal state resistance.

When a dc voltage is applied across the junction, the phase difference oscillates according to

$$\frac{d(\theta_1 - \theta_2)}{dt} = \frac{4\pi eV}{h} \quad . \tag{1.12}$$

Now, the current through the junction becomes

$$I_S = I_C \sin(\omega_J t + \phi_0), \qquad \phi_0 \text{ being an initial phase.} \tag{1.13}$$

The frequency at which the junction current oscillates, is given by

$$f_J = \frac{\omega_J}{2\pi} = \frac{2eV}{h}. \tag{1.14}$$

This effect is called the ac Josephson effect. ω_J, which is also known as the characteristic frequency ω_C, depends on the product of the critical current I_C and the normal resistance R_N, known as the characteristic voltage V_C. In the presence of a magnetic field, the Josephson relation can be written in terms of the gauge-invariant phase difference ϕ,

$$I_S = I_C \sin(\phi), \text{ where } \phi = \theta_1 - \theta_2 - \frac{2\pi}{\Phi_0}\int_1^2 \vec{A}.d\vec{l} \ . \tag{1.15}$$

1.4.3 Josephson coupling energy and Josephson inductance

The work done on a junction to change its phase from ϕ_1 to ϕ_2 is given by

$$E = \frac{\Phi_0 I_C}{2\pi}(\cos\phi_1 - \cos\phi_2). \tag{1.16}$$

This suggests that the potential energy of the Josephson junction can be written as

$$E_J = \frac{\Phi_0 I_C}{2\pi}(1 - \cos\phi) = E_C(1 - \cos\phi), \tag{1.17}$$

where E_C is known as the Josephson coupling energy.
From relations (1.10), (1.12) and (1.15), we can obtain

$$V = \frac{h}{4\pi e I_C \cos\phi}\frac{dI}{dt} = L_J \frac{dI}{dt}, \tag{1.18}$$

where L_J is the Josephson inductance. For weak signals, a Josephson junction is equivalent to a non-linear inductance.

1.4.4 Equivalent circuit-RCSJ model

A real junction (figure 1.3) is considered as an ideal junction connected in parallel with a resistor, R representing the normal electron current and a capacitor, C contributing the displacement current. This model describing the current flow through a practical junction is known as the Resistively and Capacitively Shunted Junction (RCSJ) model.

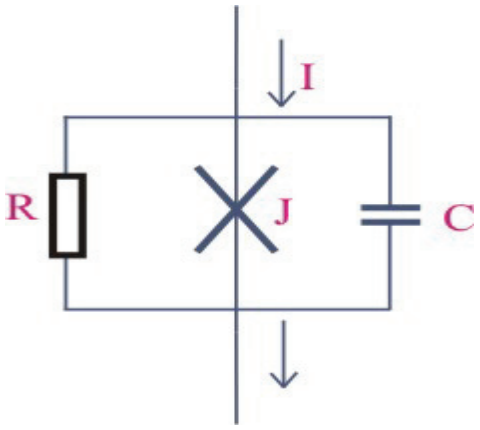


Figure 1.3: Equivalent circuit of a Josephson junction.

Using equations (1.12) and (1.15), the total current through the real junction becomes

$$I_{tot} = I_C \sin(\phi) + \frac{h}{4\pi eR}\frac{d\phi}{dt} + \frac{hC}{4\pi e}\frac{d^2\phi}{dt^2}. \tag{1.19}$$

This is a non-linear, second order differential equation. With the introduction of the dimensionless notation $\tau = \frac{1}{\tau_J} = \frac{2\pi I_C Rt}{\Phi o}$, equation (1.19) becomes

$$\beta_C \frac{d^2\phi}{d\tau^2} + \frac{d\phi}{d\tau} + \sin\phi = \frac{i_{tot}}{i_C}. \tag{1.20}$$

$$\text{where } \beta_C = \frac{RC}{\tau_J} = \frac{2\pi R^2 I_C C}{\Phi_0} \tag{1.21}$$

β_C is the damping parameter introduced by Stewart [18] and McCumber [19].

Strong damping β_C << 1:

In the limit of strong damping, the junction model is considered as a parallel connection of an ideal junction and a resistor. Now equation (1.20) becomes

$$\frac{i_{tot}}{i_C} = \sin\phi + \frac{d\phi}{d\tau}. \tag{1.22}$$

If $i_{tot} < I_C$, all the current is flowing through the junction without developing any voltage. We get

$$\phi = \sin^{-1}\left(\frac{i_{tot}}{i_C}\right) \text{ for } i_{tot} \le I_C. \tag{1.23}$$

If $i_{tot} > I_C$, equation (1.22) becomes

$$d\tau = \frac{1}{\left(\frac{i_{tot}}{I_C} - \sin\phi\right)} d\phi. \tag{1.24}$$

By solving equation (1.24), the average dc voltage across the system is given by

$$\langle v(t)\rangle = i_{tot} R\sqrt{1-\left(\frac{I_C}{i_{tot}}\right)^2} \quad \text{for } i_{tot} \geq I_C \,. \tag{1.25}$$

When the applied current exceeds the critical current I_C, part of the current is going through the resistor which generates a voltage causing the current through the junction to oscillate with the Josephson frequency. The resulting I-V characteristic is a non-hysteretic one as shown in figure 1.4a. This model is also known as the Resistively Shunted Junction model (RSJ model).

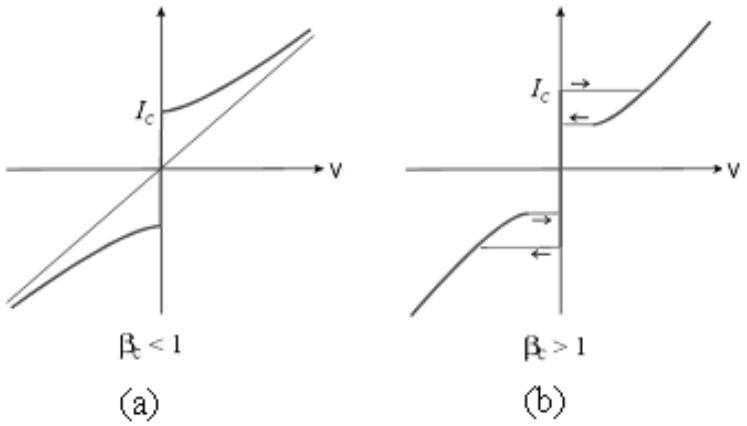


Figure 1.4: a) I-V characteristics of an over-damped junction and (b) of an under-damped junction.

Weak damping β_C >>1:

In the limit of weak damping, due to the large capacitance, the system dynamics is determined by the capacitor and the resistor in the circuit. There is no direct solution for this condition. Equation (1.20) can be solved numerically. When the applied current is increased from 0 to I_C, it flows through the junction itself. When the current exceeds I_C, a voltage appears as part of the current goes through the resistor. If one decreases the current below I_C, the junction still stays in a finite voltage state because the capacitive term dominates the dynamics of the system. Therefore, the I-V curve (see figure 1.4b) becomes hysteretic.

To understand the non-linear behavior of the Josephson junction, two mechanical analogs are used: a single pendulum driven by an external torque and a ball in a washboard-like potential.

The basic equation describing the motion of a pendulum (figure 1.5) which is similar to the equation of the Josephson dynamics is written as

$$\mathrm{M}\frac{d^2\phi}{dt^2} + D\frac{d\phi}{dt} + mgl\sin\phi = T \,. \tag{1.26}$$

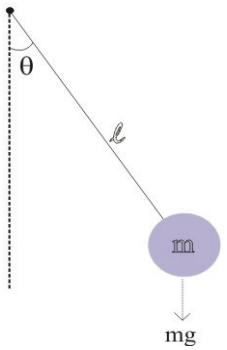


Figure 1.5: Pendulum analog of a Josephson junction. The angle θ corresponds to the junction phase ϕ and a 2π rotation corresponds to change of flux by Φ_0.

M is the moment of inertia of the pendulum corresponding to the capacitance of the junction. The angle θ is the angle of the rotation of the pendulum which is the analog of the phase difference of the junction. The applied torque T is identified as the driving current i_{tot} and the damping constant D corresponds to the conductance $(1/R)$ of the junction. The situation $i_{tot} < I_C$ is similar to a condition in which the applied torque T is less than the critical torque necessary to raise the pendulum to an angle of π/2. Now, if the pendulum is over-damped, a small kick results in one complete rotation and then it stays at its sub-critical position. A short pulse applied to an over-damped junction in its sub critical state ($i_{tot} < I_C$) causes its phase difference to make a 2π rotation. According to the Josephson second relation, this corresponds to the generation of a single flux quantum pulse (SFQ) of quantized area given by

$$\int V dt = \Phi_0 = h/2e = 2.07 \times 10^{-15} Wb\,. \tag{1.27}$$

The generation, reproduction and transport of SFQ pulses and their processing to realize useful functions form the basis of RSFQ logic circuits which will be described in more detail in chapter 3.

1.4.5 The dc-SQUID

A parallel connection of two Josephson junctions forms a device called SQUID (Superconducting Quantum Interference Device). The difference between the gauge invariant phases ϕ_1 and ϕ_2 can be found by integrating $\Delta\theta$ along a contour C as shown in figure 1.6.

$$\phi_1 - \phi_2 = 2n\pi + \frac{2\pi\Phi}{\Phi_0}\,. \tag{1.28}$$

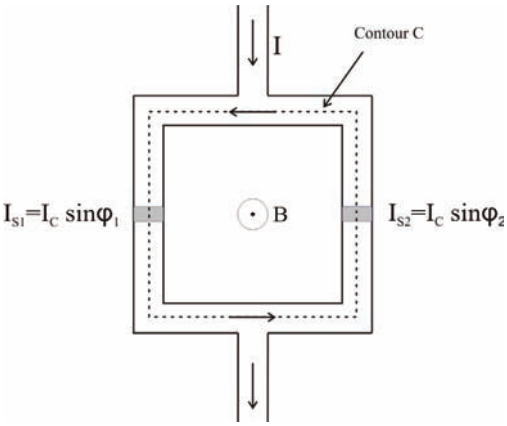


Figure 1.6: DC-SQUID formed by two Josephson junctions intersecting a superconducting loop.

If one assumes the junctions to be identical, the total current, I_{Sq} and the total flux, Φ are given by the following equations [20]

$$I_{Sq} = 2I_C \cos\left(\frac{\pi\Phi}{\Phi_0}\right)\sin\left(\phi_1 + \frac{\pi\Phi}{\Phi_0}\right). \tag{1.29}$$

$$\Phi = \Phi_{ext} - LI_C \sin\left(\frac{\pi\Phi}{\Phi_0}\right)\cos\left(\phi_1 + \frac{\pi\Phi}{\Phi_0}\right). \tag{1.30}$$

Equations (1.29) and (1.30) completely describe the behavior of the SQUID.

Limit of $LI_C << \Phi_{ext}$

When the inductance of the SQUID is negligible, the total flux is equal to the applied flux.

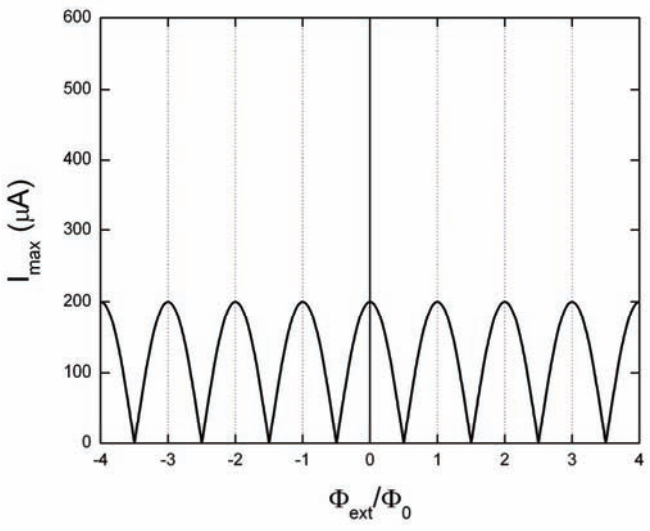


Figure 1.7: Example of a relation between I_{max} and the externally applied flux in the limit $LI_C << \Phi_{ext}$

The maximum value of the supercurrent of the SQUID $I_{\max}$ is given below by

$$I_{\max} \approx 2I_C \left| \cos \frac{\pi \Phi}{\Phi_0} \right|, \tag{1.31}$$

where $I_{\max}$ is a periodic function of the applied flux as shown in figure 1.7.

Limit of $LI_C >> \Phi_{ext}$

In the large inductance limit, the flux produced by the screening current can not be neglected. The screening current tends to compensate the external flux for a large inductance. Let us define a screening parameter β_L defined by the relation, $\beta_L = \frac{2LI_C}{\Phi_0}$.

The relation between the total flux of the SQUID and the applied flux is given by

$$\Phi_{ext} = \Phi + LI_C \sin\left(\frac{\pi \Phi}{\Phi_0}\right). \tag{1.32}$$

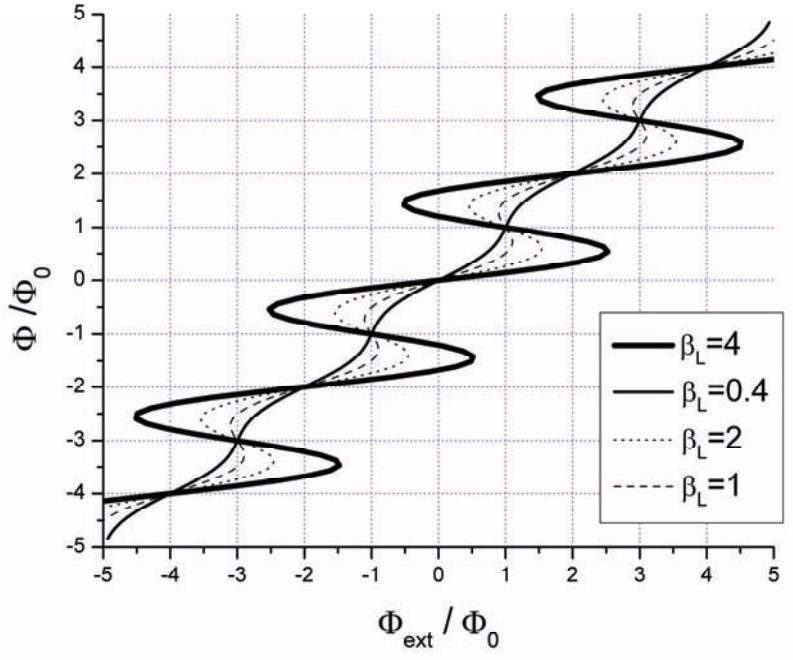


Figure 1.8: The total flux versus the applied flux for a SQUID with two identical junctions for different values of β_L.

A multi-valued relationship (figure 1.8) between Φ and Φ_{ext} exists for large β_L. The screening parameter should be less than unity to avoid magnetic hysteresis [21].

References

1. J. Bardeen, L. N. Cooper and J. R. Schrieffer, "Theory of superconductivity," Phys. Rev., **108** (1957) 1175.

2. B. D. Josephson, "Possible new effect in superconductive tunneling," Phys. Lett. **1** (1962) 251.

3. J. G. Bednorz and K. A. Muller, "Possible high T_C superconductivity on Ba-La-Cu-O system," Z.furPhys., **64** (1986) 189.

4. M. K. Wu, J. R. Ashburn, C. J. Torng, P. H. Hor, R. L. Meng, L. Gao, Z. J. Huang, Y. Q. Wang, C. W. Chu, "Superconductivity at 90K in a new mixed-phase Y-Ba-Cu-O compound system at ambient pressure," Phys. Rev. Lett., **58** (1987) 908.

5. H. Hilgenkamp, J. Mannhart, "Grain boundaries in high-Tc superconductors," Reviews of Modern Physics, **74** (2002) 485.

6. J. Gao, W. A**.** M. Aarnink, G. J. Gerritsma and H. Rogalla, "Controlled preparation of all high-T, SNS-type edge junctions and dc-SQUIDS", Physica C, **171** (1990)126.

7. B. H. Moeckley and K. Char, "Properties of interface-engineered high Tc Josephson junctions," Appl. Phys. Lett., **71** (1997) 2526.

8. K. K. Likharev, O. A. Mukhanov and V. K. Semenov, "Resistive single flux quantum logic for the Josephson-junction technology," in **SQUID'85**, W. de Gruyter, Berlin, 1103 (1985).

9. K. Likharev, O. Mukhanov, V. Semenov, "Ultimate performance of RSFQ logic circuits," IEEE. Trans. Mag., **23** (1987) 759.

10. Y. Chong, C. J. Burroughs, P. D. Dresselhaus, N. Hadacek, H. Yamamori, and S. P. Benz, " Practical High-Resolution Programmable Josephson Voltage Standards Using Double- and Triple-Stacked $MoSi_2$-Barrier Junctions," IEEE. Trans. Appl. Supercond., **15** (2005) 461.

11. A. H. Sonnenberg, G. J. Gerritsma, and H. Rogalla, "Balanced comparator fabricated in ramp edge technology," *Physica C*, **326** (1999) 12.

12. A. H. Sonnenberg, I. Oomen, H. Hilgenkamp, G. J. Gerritsma, and H. Rogalla, "Sigma-Delta A/D converter in HTS ramp edge technology," IEEE Trans. Appl. Supercond., **11** (2002) 200.

13. Y. Tarutani, Y. Ishimaru, H. Wakana, S. Adachi, K. Nakayama, Y .Oshikubo, O. Horibe, Y. Morimoto, and K. Tanabe, "Fabrication and Logic Operation of Oxide SFQ-Circuit-Components," IEEE Trans. Appl. Supercond., **15** (2005) 376.

14. Z.G Ivanov, V. K. Kaplunenko, E A Stepantsov, E Wikborg and T Claeson, "An experimental implementation of high-T,-based RSFQ set-reset trigger at 4.2 K," Supercond. Sci. Technol. **7** (1994) 239.

15. Contributions ASC 2002 and 2004 from A. Kleinsasser *et al*.

16. H. Hilgenkamp and J. Mannhart, "Mechanisms controlling interface-properties in High-Tc Superconductors," IEEE. Trans. Appl. Supercond., **9** 3405 (1999).

17. V. Ambegaokar, A. Baratoff, "Tunneling between superconductors," Phys. Rev. Lett., **10** (1963) 486 (Erratum: **11** (1963) 104).

18. W. C. Stewart, "Current-Voltage characteristics of Josephson junctions," Appl. Phys. Lett., **12** (1968) 277.

19. D. E. McCumber, "Effect of ac impedance on dc Voltage -Current characteristics of superconductor weak-link junctions," J. Appl. Phys., **39** (1968) 3113.

20. T. P. Orlando and K. A. Delin, "Foundation of applied superconductivity," Addison-Wesley publishing company, 1991.

21. M. Tinkham, "Introduction to Superconductivity," second edition, McGraw-Hill book Co., New York, 1975.

Chapter 2

HTS junction technology

2.1 HTS junctions

HTS junctions have an $I_C R_N$ product higher than that of low temperature superconducting (LTS) junctions based on niobium material. This opens the possibility to fabricate high speed SFQ circuits using HTS junction. Operating at liquid nitrogen temperature can reduce the cooling cost. Generally, these junctions are over-damped junctions with non-hysteretic I-V characteristics described by the resistively shunted junction model. HTS junctions require fully epitaxial multilayer structures. The spread in the critical current has to be low to realize complex, integrated circuit in HTS technology. The most commonly used HTS junctions are bi-crystal grain boundary junction, step edge junction, ramp type junction and interface engineered junction.

Bi-crystal grain boundary junctions are fabricated by the epitaxial growth of a HTS film on a bi-crystal substrate [1]. Grain boundary junctions are used in SQUID applications due to the low 1\f noise value [2]. The bi-crystal junction technology is not useful for integrated circuits, because junctions can not be placed freely anywhere on a chip.

In step edge junctions, the angle of the step edge fabricated into the substrate should be high enough to form grain boundaries at both upper and lower edges when an epitaxial HTS film is grown on top. Due to the low reproducibility of step edge junctions, they are not useful for RSFQ circuits [2].

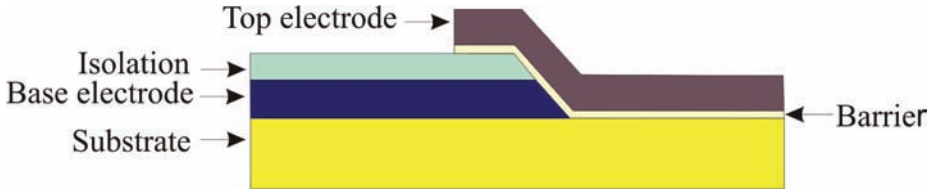


Figure 2.1: Ramp type junction geometry.

HTS ramp type junctions utilize charge transport along the crystallographic ‘a’ or ‘b’ axis directions across a thin barrier. A simple geometry of a ramp type junction is shown in figure 2.1. The coherence length along the ‘a’ and ‘b’ direction is larger than that along the ‘c’ direction. A ramp edge along the ‘a’ or ‘b’ axis is formed on the c axis oriented bi-layer composed of a superconducting thin film and an isolation layer. Epitaxial growth of a thin barrier and a top superconducting electrode over the ramp edge form the junction [3]. Junctions can be placed freely along the a-b plane using rotational etching of the ramp, which can increase the density of junctions in a device. A short coherence length requires a highly uniform, thin and smooth barrier material. Inter-

diffusion between the layers affects the stoichiometry of the composition at the interface. The critical current density can be controlled by varying the barrier thickness.

Interface engineered junctions eliminate the deposition of artificial barriers on the ramp edge. A surface-modified barrier is formed on the ramp edge by argon ion milling, followed by annealing in vacuum or in low oxygen pressure [4]. An I_C spread less than 10% has recently been reported for a 1000 junctions array [5].

2.2 Substrate for HTS electronics

For epitaxial growth, substrates should have a close lattice match with the films. Additionally, a large difference in thermal expansion coefficient might produce cracks in the film [6]. Chemical reactions between the substrate and the film will result in a deviation from the desired phase growth. Any contamination and irregularities on the substrate surface affect the quality of the deposited film. We are using single crystal strontium titanate ($SrTiO_3$ or STO) or magnesium oxide (MgO) substrates for the HTS junction fabrication.

STO has a perovskite structure and exists in cubic form with a lattice parameter a=3.905 Å. STO has a good lattice match to most of the HTS perovskite materials. A substrate, as received from the supplier is not suitable for direct deposition. Single terminated and atomically flat substrates are beneficial for the epitaxial growth of multilayer structure with low roughness [7].

STO's high dielectric constant (300) makes it unsuitable for high frequency applications. A very low dielectric constant (around 10) and the low cost compared to STO make MgO a more suitable substrate for junctions for high frequency applications. Efforts have been made to grow YBCO (Yttrium Barium Copper Oxide) thin films directly on an MgO substrate, but the quality of the film is not as good as deposited on an STO substrate. The deposited films showed a degraded critical temperature and critical current density. An MgO substrate has a cubic structure with a lattice parameter of 4.216 Å. A large lattice mismatch between the a-b axis of the YBCO film and the MgO substrate (more than 8%) causes the formation of defects and grain boundaries in the deposited film. With the introduction of an STO buffer layer on the substrate, high quality DBCO and YBCO can be deposited epitaxially [8].

2.3 NBCO thin film preparation and characterization

2.3.1 Introduction

YBCO is widely used as an electrode material for junctions. YBCO thin films can be grown with a transition temperature of 90 K, close to their bulk value. Recently, NBCO (Neodymium Barium Copper Oxide) obtained a lot of attention due to its higher T_C than YBCO. Melt processed NBCO shows a T_C above 96 K [9]. This compound also shows a high critical current density at 77 K under applied magnetic field. This leads researchers to have a lot of interest in studying its properties for different applications.

A unit cell of a NBCO material is shown in figure 2.2. The NBCO system forms a solid solution with the formula $Nd_{1+x}Ba_{2-x}Cu_3O_{7-\delta}$. Since the ionic radius of Ba^{2+} is larger than that of the neodymium ion, the solubility of Nd^{3+} on the Barium site is highly favorable in the NBCO compound. The substitution of Nd^{3+} for Ba^{2+} influences its properties such as its crystal structure, growth mode and superconducting properties.

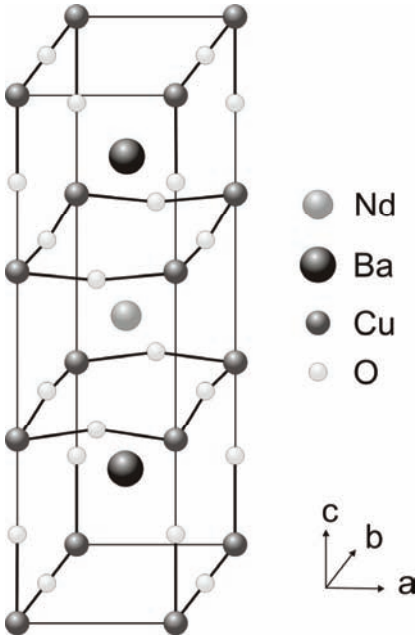


Figure 2.2: Basic unit cell of NBCO.

It is supposed that the hole concentration in the CuO_2 plane is responsible for the p-type superconductivity in the RBCO system. Substitution of Nd^{3+} for Ba^{2+} reduces the hole concentration and decreases the T_C of the material. However, it enhances the smoothness of the deposited film making it suitable for multilayer structures [10].

The dependence of the properties and structure of NBCO on cation disorder was studied by many groups [11-13]. The effect of Nd substitution on the crystal structure was studied by Takita *et al*. [14] using x-ray diffraction. The NBCO compound is orthorhombic if x is near 0. When the value of x is increased, around x=0.2, the compound becomes tetragonal. The transition temperature, which has its maximum value around x=0, is decreasing with the increase of neodymium doping. Superconductivity disappears when x is above 0.4. This proves that there is a relation between the hole concentration and the superconducting properties. The deposition parameters and the target composition have therefore, to be selected carefully for the growth of NBCO thin films with controlled properties.

2.3.2 Deposition method

A number of reports exist on the preparation of NBCO thin films by magnetron sputtering [15, 16], pulsed laser deposition [20-22] and other deposition methods. An extensive study was made by Salluzzo *et al*. [17] on the growth of NBCO films from targets with different cationic ratios. The growth of an NBCO film from a stoichiometric target is different from that of a Neodymium-rich target. In the case of stoichiometric films on STO, it starts to grow as islands and around a thickness of 5 unit cells, 2D nucleation and the coalescence of 2D islands take place. Above 12 unit cell thickness, the film becomes rough and forms multiple terraces due to screw or half-loop dislocations. For the Neodymium rich film, 3D growth has not been observed even for a 100 nm thick film.

Mori *et al*. [18] obtained contradictory results: Films deposited using a stoichiometric target showed a low roughness. The substrate temperature used was 720^0C. The target material composition, partial oxygen pressure and substrate temperature have a large influence on the properties of the deposited film.

Bae *et al*. [19] studied pulsed laser deposited NBCO thin films by using micro-Raman spectroscopy. Different oxygen pressures (100-800 mTorr) at a substrate temperature of 800 ^{0}C were used. It was found that the film grown at higher oxygen pressure exhibits c-axis growth with less cation disorder and oxygen deficiency.

A non-stoichiometric target ($Nd_{1.12}Ba_{1.88}Cu_3O_{7-\delta}$) was used for our study. We are using an RF magnetron sputter system equipped with a load-lock arrangement for the deposition. A load-lock helps to transfer the substrate to the high-vacuum chamber without breaking the vacuum. We use both STO and MgO substrates for the deposition. Mostly MgO substrates were used because of their low dielectric constant, suitable for high frequency applications. Substrates were cleaned ultrasonically by using acetone and ethanol before the deposition. They are glued carefully on the heater plate by silver paste to ensure a uniform contact between the heater and the substrate. They are heated in the open air for a few minutes to dry the silver contact with the heater. Then the heater is transferred to the high vacuum system using the load-lock. The substrate is heated to the temperature at which the material is going to be deposited. When the background pressure reaches a value less than 1×10^{-6} mbar, the system is ready for deposition. The partial pressure of argon and oxygen for the deposition depends on the materials to be deposited. The substrate is kept in an off-axis position to avoid the bombardment with energetic particles, which can damage the deposited film. A disadvantage of using an off-axis position is the reduction in the sputtering rate. Cold water flow behind the target cools the target during deposition. After deposition, an annealing procedure at high oxygen pressure is typically performed in order to obtain the required superconducting phase of the deposited film.

2.3.3 Growth on STO

For the NBCO deposition, we used 10×5 mm^2 STO substrates and the substrate temperature was kept at 810 ^{0}C during deposition. A 200 nm thick NBCO layer was grown at a total pressure of 0.35 mbar with a partial oxygen pressure of 0.02 mbar. We have studied the crystallinity and smoothness of NBCO layers deposited on both STO and MgO substrates using X-ray diffraction and Atomic Force Microscopy (AFM).

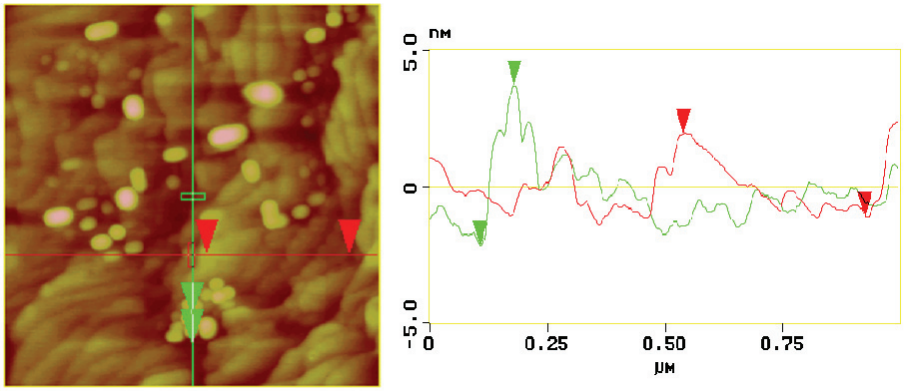


Figure 2.3: AFM image and cross section analysis of the surface of an NBCO film on STO.

The grown films are relatively smooth with a maximum peak to peak value less than 5 nm. From the AFM picture (figure 2.3), we have observed small outgrowths with dimensions less than a nanometer. There are a number of small terraces on the film with sub-unit cell height. There are no other defects on the deposited films. Figure 2.4 shows a typical transition curve of a NBCO film deposited on a STO substrate. The critical temperature, T_C (R=0) of the films is around 88-91 K, with a superconducting transition width of 3.5 K.

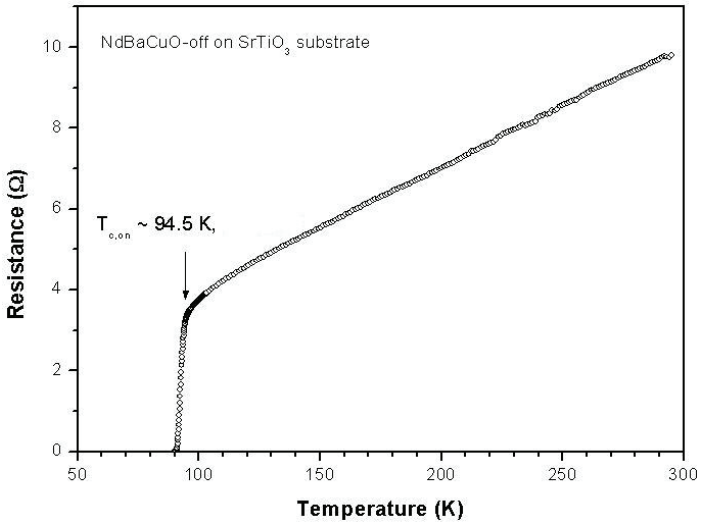


Figure 2.4: Resistance versus temperature curve of a 200 nm NBCO film deposited on STO.

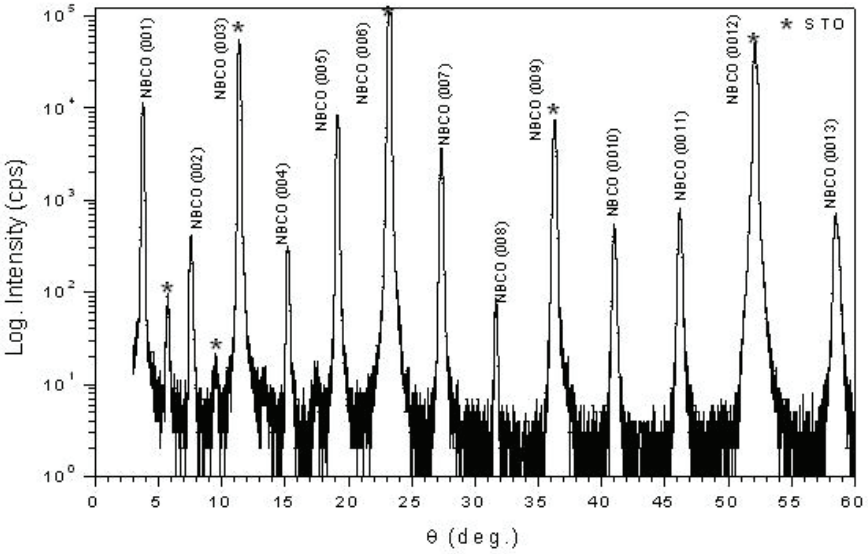


Figure 2.5: XRD spectra of a 200 nm thick NBCO film on STO.

X-ray diffraction (XRD) results of an NBCO film grown on STO is shown in figure 2.5. From this picture, only the (00n) reflections are seen. It is therefore confirmed that the grown film is highly c-axis oriented. The roughness was found to increase for films deposited at temperatures lower than 810 ^{0}C.

2.3.4 Growth on STO buffered MgO

We use a thin STO buffer layer before the deposition of NBCO on an MgO substrate to avoid a large lattice mismatch between the NBCO and the MgO. The buffer layer also has a comparable thermal expansion coefficient with the substrate. We were able to grow highly smooth STO layers (figure 2.6) with an average roughness of about 0.4 nm for a thickness of 35-40 nm.

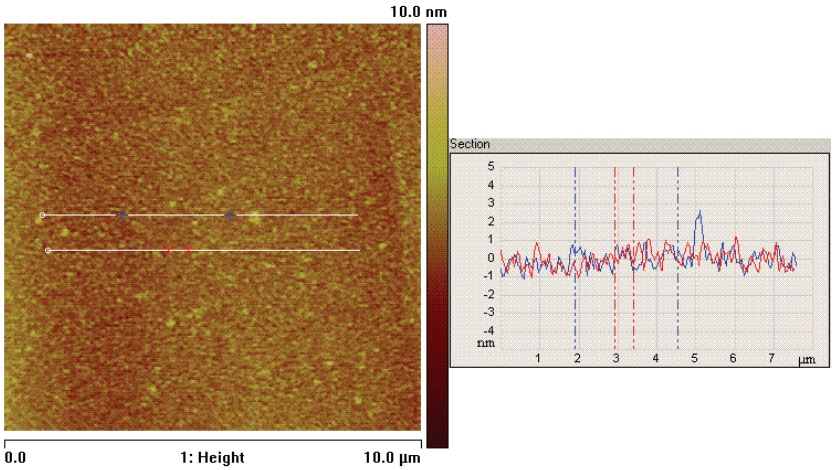


Figure 2.6: AFM image and cross section analysis of a 40 nm thick STO buffer layer on an MgO substrate.

After the deposition of the buffer layer, a 150 nm thick NBCO thin film is deposited in-situ at 820 ^{0}C. From AFM studies (figure 2.7), we see that the film is very smooth with a surface roughness of 1-3 nm.

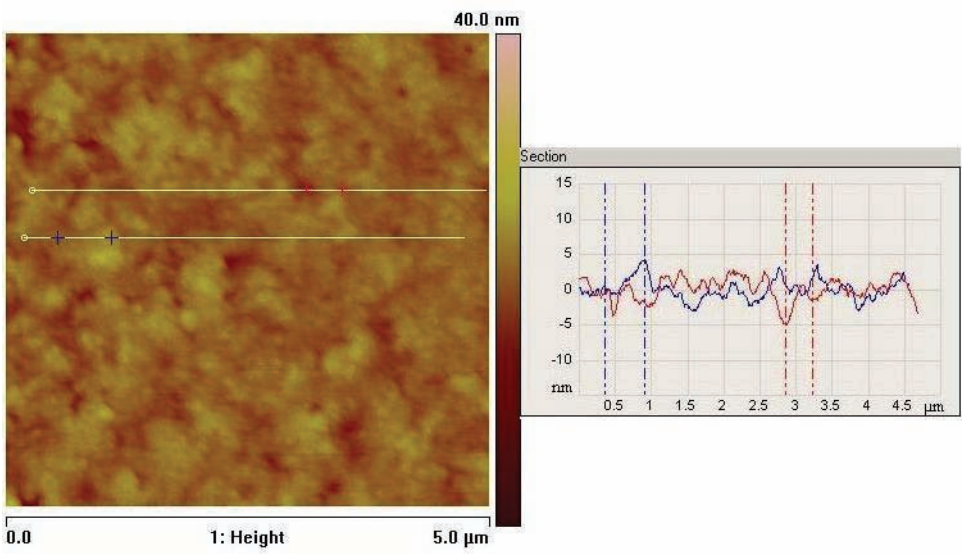


Figure 2.7: AFM image and cross section analysis of a 150nm thick NBCO layer on $SrTiO_3$ buffered MgO substrates.

NBCO films deposited on top of the buffer layer show good superconducting properties with critical temperatures T_C (R=0) of 90-92 K, and superconducting transition widths of ΔT_C ~ 3 K. Figure 2.8 shows the transition curve of a NBCO film deposited on a STO buffered MgO substrate.

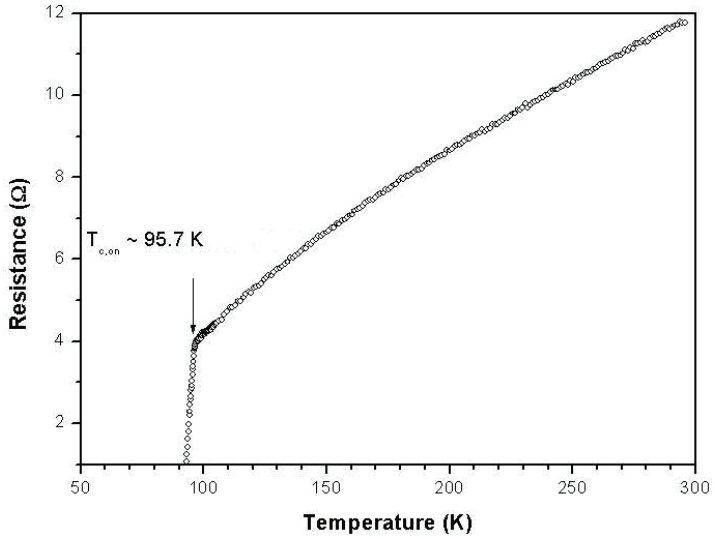


Figure 2.8: Resistance versus temperature curve of a 150 nm NBCO film deposited on STO buffered MgO.

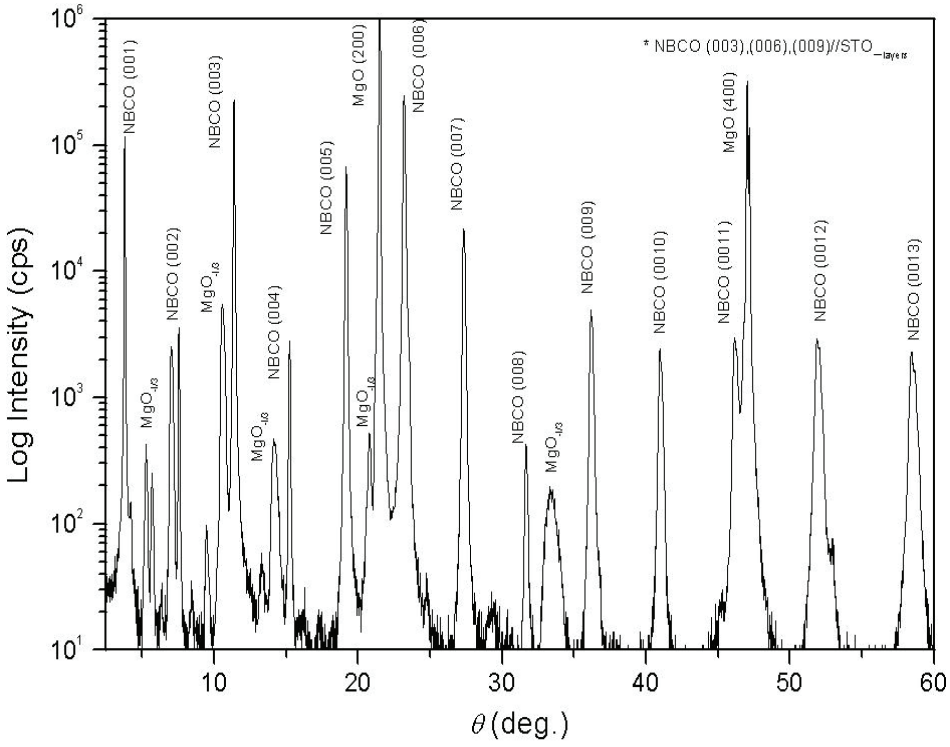


Figure 2.9: XRD spectra of 200 nm thick NBCO film on the STO buffered MgO substrate.

XRD result (figure 2.9) shows that both the STO and the NBCO layers grow epitaxially on the MgO substrate with their c-axis perpendicular to the substrate surface. The optimum deposition conditions for a NBCO thin film are shown in table 2.1

Substrate	MgO with 35-40 nm thick STO buffer layer
Deposition	Off-axis RF magnetron sputtering
Target	$Nd_{1.12}Ba_{1.88}Cu_3O_{7-\delta}$
Pressure	0.35 mbar with 20:1 Argon and Oxygen gas mixture and a small amount of water vapour.
Substrate temperature	820 ^{0}C
Annealing	600^{0}C for 30 minutes & 450^{0}C for 60 minutes at 700 mbar oxygen pressure
T_C	89-90 K

Table 2.1: Deposition parameters of the NBCO film on the STO buffered MgO substrate

2.3.5 Surface stability

Nowadays, high quality NBCO films can be grown by different techniques. For applications such as junction technology, atomically smooth surfaces without any degradation are required. In order to avoid this, one has to investigate the surface stability against different environments.

Badaye *et al*. [23] reported pulsed laser deposited films having a thickness of about 100nm with an average roughness of less than 1.5 nm. He observed a degradation of the surface of films deposited under non optimal conditions. It was claimed that no change in the surface morphology of the optimally grown film was observed after exposure in air for 10 days.

Ting *et al.* [24] studied the surface stability of a laser ablated film exposed in high humid air using AFM and STM studies. A 100 nm thick film had well connected grains having concentric rings (spirals) due to a 2-dimensional island growth mode. After 2 hours of exposure in highly humid air, they observed places where the concentric rings disappeared with newly formed convex spots. They found that the BaO-layer at the edges of the grain boundaries might react with moisture forming $Ba(OH)^2$, which can react with CO_2 forming $BaCO_3$ and H_2O. The resulting compounds can migrate and form convex spots with the copper oxide layer. They also found that the normal resistance increased after the exposure because of the degradation of top layers.

We have observed no degradation in the T_C of NBCO films, when kept in dry conditions for a few months. Long annealing in oxygen after the deposition does affect the T_C of the film. We observed a reduction of T_C by 2K if the annealing time was increased by 2 hours.

2.4 Isolation layers and barrier material

An isolation layer must provide not only a good insulation between the superconducting layers but also provide a way to recover the superconductivity of the bottom layer during annealing. We tried to use a combination of a Ga-doped $PrBa_2Cu_3O_7$ (PBCGO) and $SrTiO_3$ as isolation layers. A SEM (Scanning Electron Microscopy) picture of a PBCGO film with a thickness of about 100 nm is shown in figure (2.11).

A SEM (Scanning Electron Microscope) of a 100 nm PBCGO layer is shown in figure 2.10. A large roughness with outgrowths on the film surface has been observed. The height of the outgrowths varies from 20 to 90 nm. An XPS (X-ray Photoelectron Spectroscopy) analysis showed that the outgrowths are rich in copper. Since the optimizations of the deposition conditions did not improve the smoothness of the layer, the PBCGO film was replaced by an undoped $PrBa_2Cu_3O_7$ (PBCO) layer.

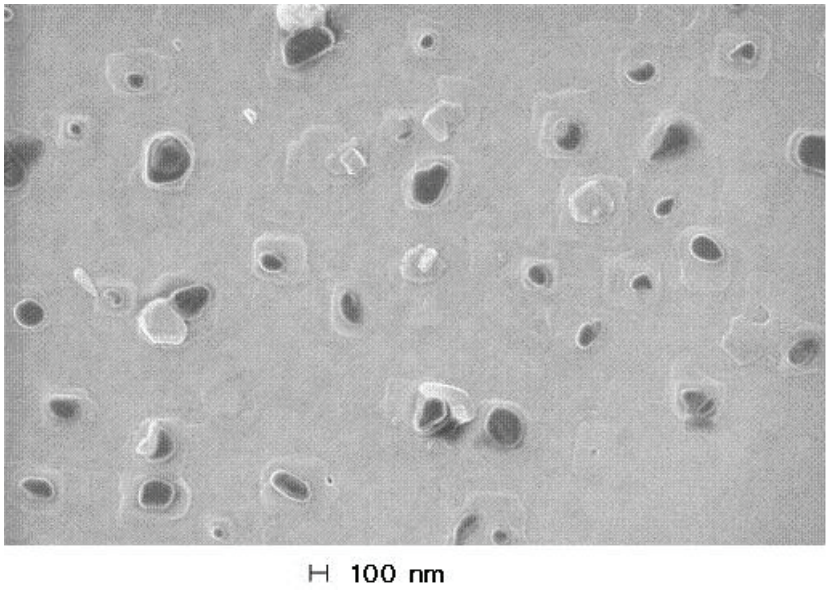


Figure 2.10: SEM image of a PBCGO film deposited on an STO-buffered MgO substrate.

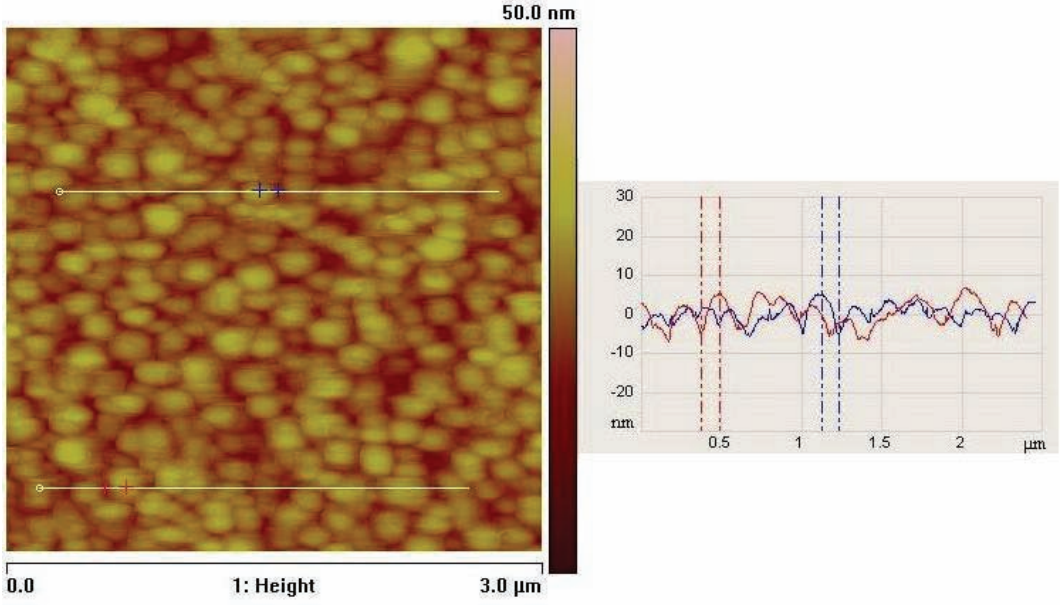


Figure 2.11: AFM image and cross section analysis of a 120 nm thick PBCO layer.

A 120 nm PBCO film deposited over a stack of 3 layers (STO buffer/NBCO/STO) (figure 2.11) showed a roughness less than 3 nm. X-Ray diffraction analysis shows a fully c-axis oriented film.

The advantage of using ramp-type junctions with an artificial barrier is that the critical current can be changed by controlling both the ramp area and the thickness of the barrier layer. A short coherence length of the HTS materials requires a thin barrier in order to obtain high critical current Josephson junctions for circuit applications. The

quality of the ramp surface influences the growth of the barrier material to be deposited. The ramp angle should be less than 45^0 to ensure epitaxial growth of the barrier layer and to avoid the growth of phases other than the desired phase. Structuring of ramps has been done by ion beam etching. Due to defects at the interface, the critical current density is decreased by the suppression of the order parameter at the interface [25]. The Microstructure of the ramp was studied extensively by Blank *et al*. and Horstmann *et al*. [28, 29]. A ramp that is well aligned with the edge of the substrate parallel to the crystal axes enhances the smoothness of the deposited barrier layer [27].

PBCO is widely used as a barrier material due to its lattice match with DBCO and YBCO [27]. It shows a semiconducting behavior. Doping PBCO with Gallium for the copper sites enhances the resistivity and thus increases the $I_C R_N$ product of the junction up to 8 mV at 4 K [30]. The transport properties of junctions with PBCGO barrier [25, 30, and 31] were studied extensively.

The barrier material has to be lattice matched with the superconducting electrode in order to grow epitaxially. The quality of the interface between the barrier and the electrode influences the transport mechanism of the junction. A different thermal expansion coefficient of a barrier material can produce defects at the interface due to stress between the barrier and the superconducting electrode producing oxygen disorder at the junction interface [26]. The effective thickness of the barrier changes with the level of impurities at the interface.

2.5 NBCO/PBCGO/NBCO ramp type junctions and SQUIDs

2.5.1 Junction fabrication

All the steps involving the fabrication of a ramp type junction with a ground plane are shown in figure 2.12. All depositions, except for the gold layer, were done by off-axis RF magnetron sputtering.

A thin buffer layer of STO was grown on top of an MgO substrate in order to ensure the epitaxial growth of subsequent layers. A 150 nm thick NBCO or DBCO ground plane was sputter deposited and patterned by standard photolithography and argon ion etching. A stack of STO/PBCO/STO layers is used as isolation to separate the ground plane from the wiring layers. Via holes were etched by using a photo resist mask wherever an electrical contact between the ground plane and other superconducting layers needed to be established. Then, an in situ deposition of a 150 nm thick NBCO or DBCO base electrode and a bi-layer of STO/PBCO were deposited to separate the base electrode from the counter electrode.

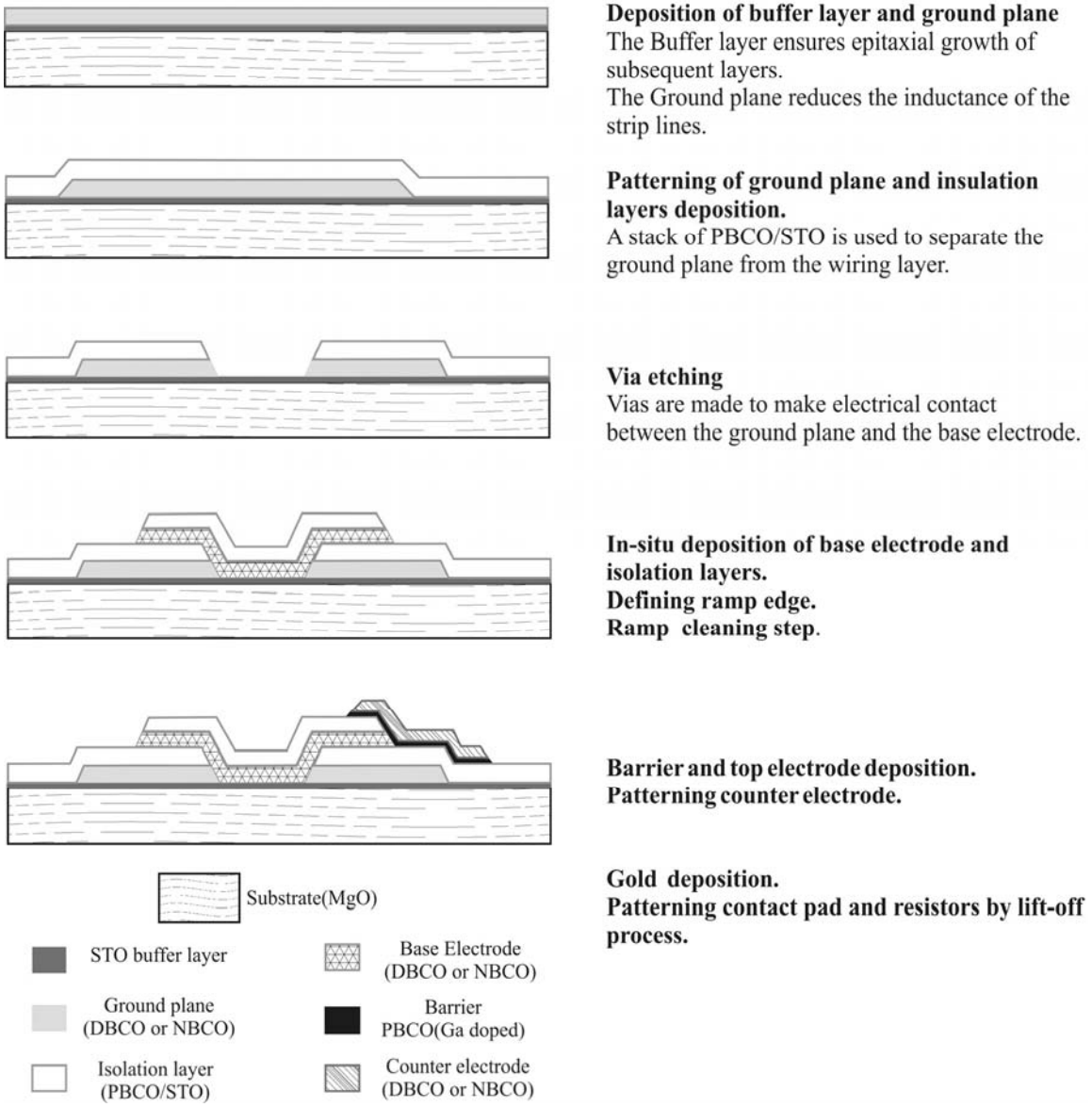


Figure 2.12: Ramp type junction process.

The base electrode was patterned and ramp edges were defined by argon ion milling. After cleaning the ramp edges by argon ion etching to remove a thin, contaminated layer, without breaking the vacuum, the sample was transported into the deposition chamber for an in situ sputter deposition of the PBCGO barrier layer and the NBCO counter electrode. The junction width and inductors were defined. Finally metallization and patterning resistors were realized by a lift-off process with DC gold sputter deposition. An optical photograph taken before the metallization process is shown in figure 2.13.

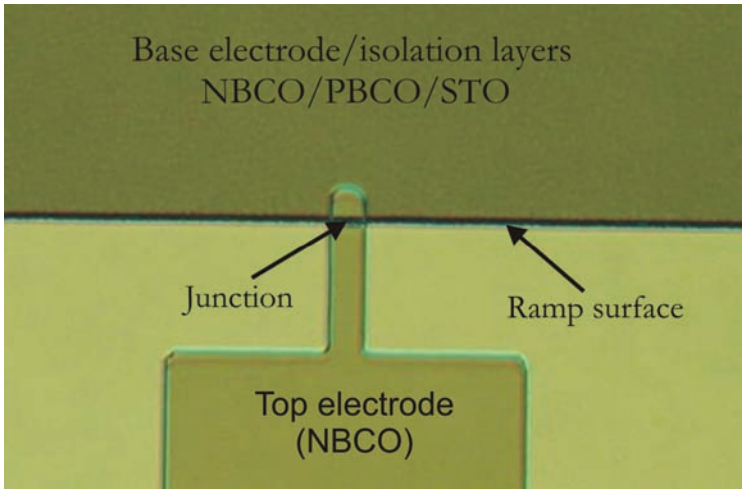


Figure 2.13: Optical photograph of a fabricated ramp type junction.

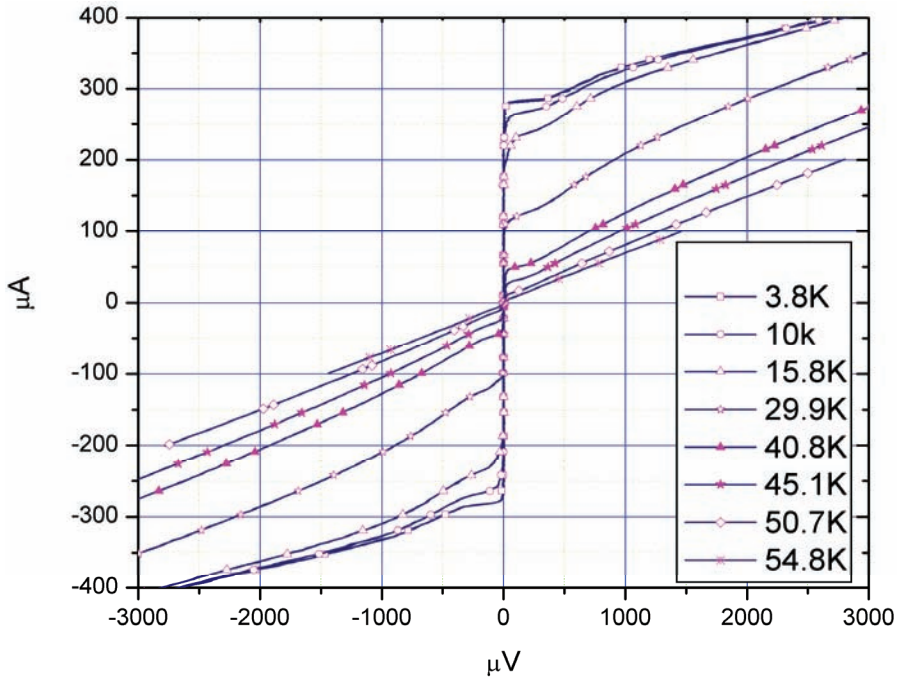


Figure 2.14: I-V characteristics of an 8 μm wide junction for different temperatures.

A typical junction I-V characteristic is shown in figure 2.14. Mostly, the junctions showed RSJ like behavior with excess current [32]. Normally a barrier thickness of 12-15 nm is used. The main source of excess current is formed by the pin holes in the ramp area. The value of the I_CR_N product is around 2 mV at 4 K. A plot of the I_CR_N product as a function of temperature of the junction with a 12 nm thick PBCGO barrier is shown in figure 2.15.

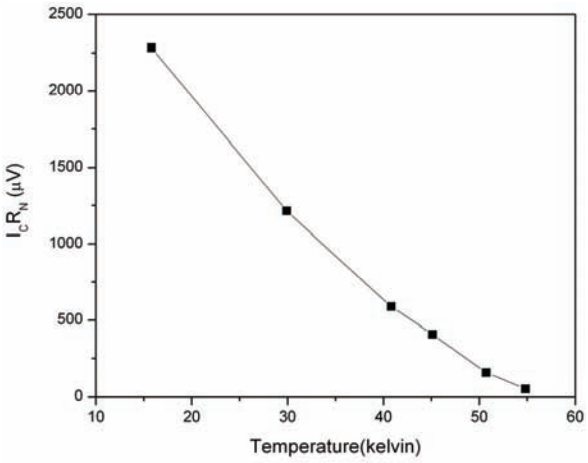


Figure 2.15: Temperature dependence of the I_CR_N product of the junction with a 12nm thick PBCGO barrier.

2.5.2 Junction reproducibility issues

Ramp etching is done by argon ion milling with an acceleration voltage of 500 V at an angle of 35^0 with respect to the film surface. After removing the photo resist, a ramp cleaning step has been taken by means of low voltage (50 V) argon ion etching to remove the contaminated surface on the ramp area. An AFM picture of a bare ramp area is shown in figure 2.16. The surface is smooth with an average roughness less than 4 nm.

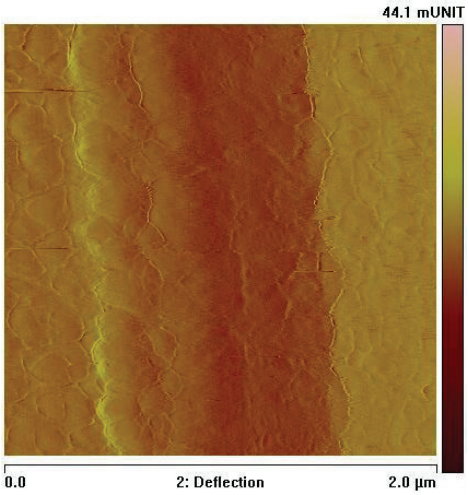


Figure 2.16: AFM image of a ramp edge.

Before the deposition of barrier and top electrode, ramp annealing has been done to recrystalize the amorphous layer on the ramp surface. The recrystalization might further increase the roughness of the barrier region which causes a spatial change in the barrier thickness and an increase in the chance of forming micro shorts between the electrodes. These effects were found to increase the spread in junction characteristics.

In order to study the variation in the critical current of the junctions in a chip, a special chip containing 48 individual junctions of 5 μm width placed in 3 rows has been fabricated. Each junction is placed 300 μm apart in a row. Mostly, within the area of 1 mm^2, junctions had $\pm(5-20)\%$ spread from their mean value. The ramp annealing steps used for the NBCO ramp are the same as those for the DBCO ramp edge. Re-optimization of the ramp annealing step might reduce the roughness of the ramp area during recrystallization. The measured T_C value of the ground plane and of the base electrode after the entire junction process is lower than that of a bare NBCO film. For a device with a degraded base electrode, the junction I_C showed a lower value for the same barrier thickness. The effective barrier thickness locally changes with the roughness of the ramp area and the quality of the interface.

A high transparency of the barrier/electrode interface can be obtained with the introduction of an interlayer in this junction type (figure 2.17). Non-stoichiometry at the ramp surface can exists due to the preferential etching of some of the elements. Before the deposition of the barrier layer, a thin layer of superconducting film is deposited to restore the stoichiometry of the material at the ramp edge. The thickness of the interlayer is taken in such a way that it is expected to be superconducting only in the ramp area and non-superconducting in the remaining area over the chip [33]. The interlayer ensures superconductivity at the ramp area due to its perfect lattice match. We have used a 10 nm thick NBCO layer as interlayer and a 9 nm thick PBCGO as barrier layer.

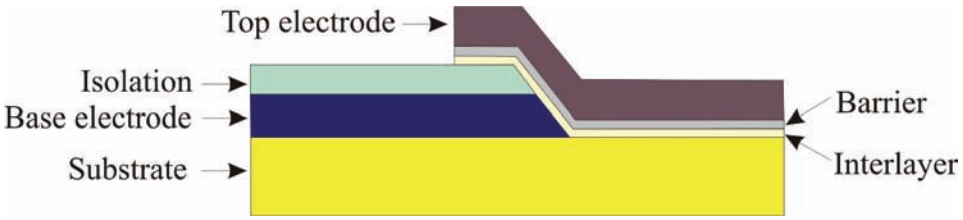


Figure 2.17: Ramp type junction with an interlayer.

All junctions showed I-V curves (figure 2.18a) with large excess current and showed a large spread in I_C. If we assume that the crystallinity of the damaged ramp area by ion milling process is not fully recovered, the effective barrier thickness is small at ramp surfaces where it is fully recovered and large at places where it is not recovered. If the ramp area is rough, there will be chances of pin holes at ramp surfaces while using a thin barrier. The same argument can also be applied to fully recovered ramp surfaces related to their roughness. Ramp annealing steps have to be investigated to study their effect of the recrystalization of the NBCO ramp surface on roughness.

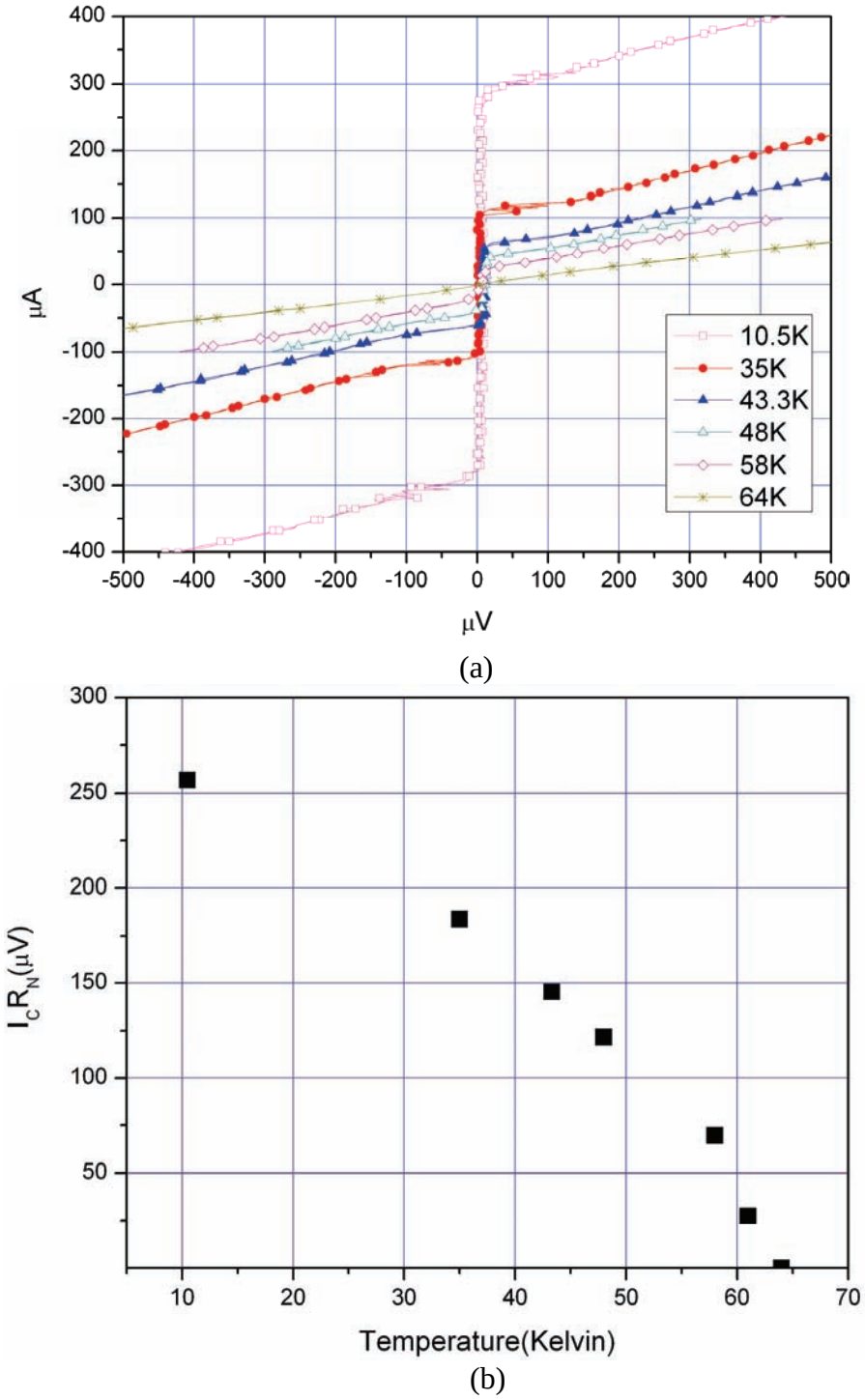


Figure 2.18: (a) IV characteristics and **(b)** the $I_C R_N$ product of a junction with a 10 nm thick interlayer at different temperatures.

A graph showing the dependence of the $I_C R_N$ product on temperature is given in figure 2.18b. The $I_C R_N$ product was less than that of a normal junction. There might be a leakage current which shunts the junction when the interlayer reaches its critical

thickness. Further study with thicker barriers is necessary to improve the quality of the junctions. The interlayer concept works well in Josephson contacts between high T_C and low T_C electrodes. In this case there is no d-wave counter electrode and the thickness of Au barrier is large compared to the roughness of ramp surface. There is also no high temperature process step after the interlayer deposition in the HTS-LTS case.

2.5.3 Direct injection SQUIDs for inductance measurements

SFQ circuits consist of SQUID loops connected in parallel or in series depending on the circuit functions. The SQUID inductance together with the critical current of the junction plays an important role in determining the timing of an SFQ pulse traveling in RSFQ circuits. So, measuring the exact value of the sheet inductance of a superconducting strip-line is necessary for the circuit design. A low value of the sheet inductance provides a large flexibility in circuit design. The inductance of a superconducting strip-line can be reduced, when a ground plane is used.

For a superconducting strip-line of width W and thickness t_1 placed at a distance h above a second superconducting ground plane of thickness t_2, the inductance per unit length [34] L is given by

$$L = \frac{\mu_0}{K(W,h,t_1)W}\left[h + \lambda_1 \coth\left(\frac{t_1}{\lambda_1}\right) + \lambda_2 \coth\left(\frac{t_2}{\lambda_2}\right)\right]. \qquad (2.1)$$

K is the fringe field factor which is nearly unity if $\frac{W}{h} \to \infty$. λ_1 and λ_2 are the London penetration depths of the respective superconducting plane of thickness t_1 and t_2.

A direct injection SQUID is used for the inductance measurements. A schematic of a direct injection SQUID is shown in figure 2.19. The voltage of a SQUID biased by a dc current I_b is modulated by sending a current I_{con} through a part of the inductance L_{con} of the squid. The product of the control current I_{con} and the inductance L_{con} corresponds to the applied magnetic field in to the SQUID loop. The inductance is evaluated by the following relation,

$$L_{con} = \frac{\Phi_0}{\Delta I_{con}}. \qquad (2.2)$$

ΔI_{con} is the modulation period. Sheet inductances are estimated by calculating the number of squares in the strip-line (forming a part of the inductance of the SQUID) through which the control current passes.

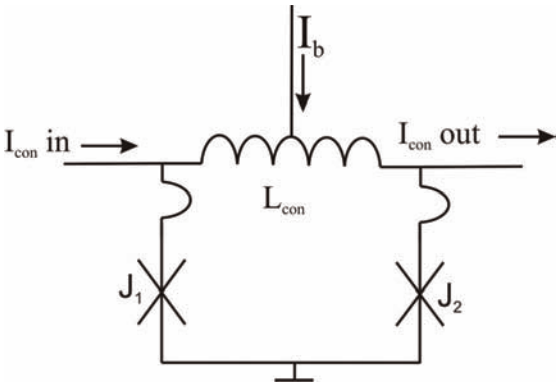


Figure2.19: Schematic of a direct injection SQUID.

A test sample was fabricated to find the sheet inductance of the base and top electrodes with a ground plane. An optical photograph of the fabricated direct injection SQUID is shown in figure 2.20.

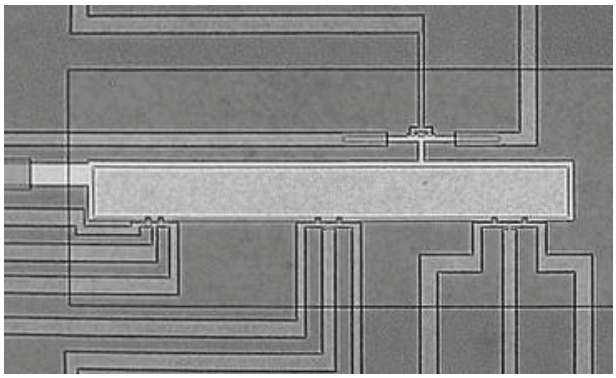


Figure 2.20: A photograph of direct injection SQUIDs fabricated with a ground plane.

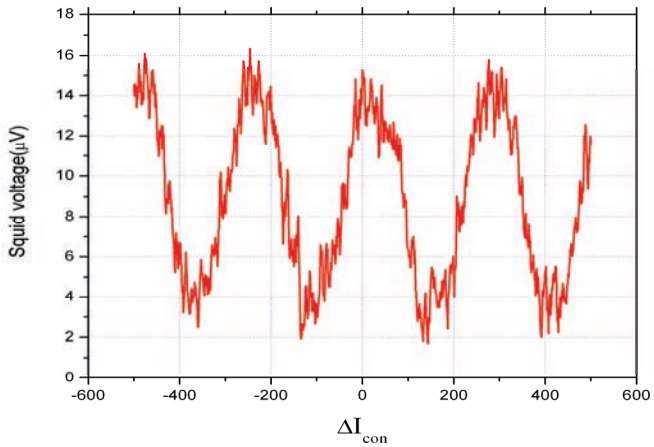


Figure 2.21: Voltage modulation as a function of control current at 30 K.

All the fabricated SQUIDs showed voltage modulation under constant bias current (figure 2.21) up to near the T_C of the junction. The value of the sheet inductance of the base and top electrode at 20K was 1.20 and 1.60 pH respectively. Below 20K, the inductance value has only a weak dependence on temperature (figure 2.22). Above 20K, the inductance increased with increasing temperature.

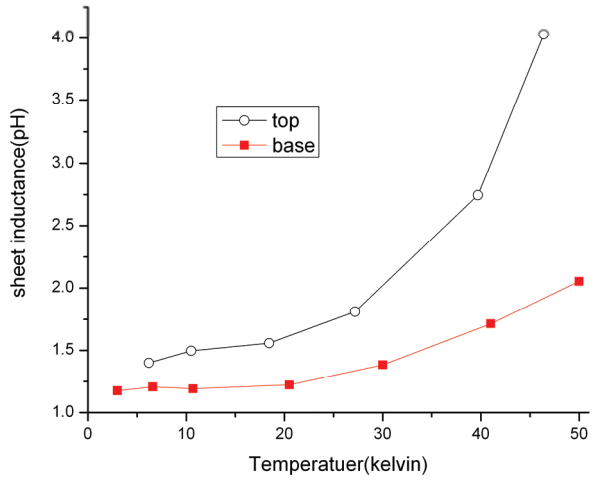


Figure 2.22: Temperature dependence of the sheet inductance of base and top electrodes fabricated with a ground plane.

The inductance of the strip-line depends on the film properties. The higher value of the inductance of the top electrode is due to an increase in the roughness of the film. In this sample, PBCGO was used as an isolation layer which showed an average roughness larger than 20 nm. Another reason for the high value of the sheet inductance might be the degradation of the superconducting properties of the ground plane and base electrode due to the thermal cycling during the process.

2.6 Conclusion

In ramp-type junctions, the active area lies on the ramp where both electrodes are separated from each other by a barrier material. Epitaxial growth of multilayer HTS thin film process is well developed. For a stack of 10 layers (including a thin barrier layer) in the junction process, an average roughness less than 5nm has been obtained. Critical steps in the junction process are the structuring of ramp (ion-milling, ramp annealing) and the growth of barrier and top electrode on the ramp area. In general, the quality of interfaces between the barrier and electrodes are degraded by the mismatches in lattice parameters, thermal expansion coefficients and chemical compatibility between barrier and electrodes and the anisotropic nature of the HTS materials.

NBCO was chosen as a superconducting electrode for its high T_C and smooth film growth. A bare thin film of NBCO deposited on STO buffered MgO shows a T_C around

90K with an average roughness around 1-3 nm. One of the main problems in the NBCO junction is the degradation of T_C (by 30-35K) of the ground plane and the base electrode. There is a problem in the restoration of superconductivity fully even for a long annealing time. This problem has not been observed in DBCO junctions.

NBCO/PBCGO/NBCO ramp type junctions have been fabricated. A ramp area with a maximum peak to peak roughness around 5 nm was obtained. A 12-15 nm thick barrier layer was used. Junctions mostly showed RSJ like behavior with excess current. A large spread in critical current was observed over a large area of the chip. The large roughness that appeared on the ramp area after the completion of the junction fabrication suggests that the roughness might be increased by the ramp annealing process and there might be a problem in the growth and nucleation of layers grown on the NBCO ramp area. Junctions with a thin superconducting layer (interlayer) before the deposition of barrier have been explored, but first results showed a large spread in I-V curves with a low $I_C R_N$ product around 200 μV at 10K. Direct injection SQUIDs have been fabricated to measure the inductance of the strip lines. Due to the degradation of the T_C of NBCO layers, the inductance values increase at a high rate above 20 K.

References

1. H. Hilgenkamp and J. Mannhart, "Superconducting and normal-state properties of $YBa_2Cu_3O_{7-\delta}$-bicrystal grain boundary junctions in thin films," Appl. Phys. Lett., **73** (1998) 265.

2. N. Klein "High frequency application of high-temperature superconductor thin film," Rep. Prog. Phys. **65** (2002) 1387.

3. J. Gao, W. A. M. Aarnink, G. J. Gerritsma and H. Rogalla, "Controlled preparation of all high-T_C SNS type edge type junctions and DC SQUIDs," Physica C, **171** (1990) 126.

4. Y. Soutome, R. Hanson, T. Fukazawa, K. Saitoh, A. Tsukamoto, Y. Tarutani and K. Takagi, "Investigation of ramp type junction with surface-modified barrier," IEEE Trans. Appl. Supercon. **11** (2001) 163.

5. H. Wakana, A. Adachi, T. Tsubone, Y. Tarutani, A. Kamitani, K. Nakayama, Y. Ishimaru, and K. Tanabe, "Fabrication of high-temperature superconducting single-flux-quantum circuits using a multilayer structure with a smooth surface," Supercond. Sci. Technol., **19** (2006) S312.

6. D. P. Norton, "Synthesis and properties of epitaxial electronic oxide thin-film materials," Material Science and Engineering, **R 43** (2004) 139.

7. G. Koster, G. Rijnders, D. H. A. Blank and H. Rogalla, "Surface morphology determined by (0 0 1) single-crystal $SrTiO_3$ termination," Physica C, **339** (2000) 215.

8. L. Michin, Q. Meng, A. H**.** Sonnenberg, G. J. Gerritsma, "$SrTi0_3$ buffer layers on MgO and Si substrates for high-Tc technology," IEEE Trans. Appl. Supercon., **9**, (1999) 1666.

9. S.I. Yoo, M. Murakami, N. Sakai, T. Higuchi, S. Tanaka, "Enhanced T_C and strong flux pinning in melt processed NdBa2Cu3Oy superconductors," Jpn. J. Appl. Phy., **33** (1994) L1000.

10. S. Bals, G. Van Tendeloo, M. Salluzzo, and I. Maggio-Aprile, "Why are sputter deposited $Nd_{1+x}Ba_{2-x}Cu_3O_y$ thin films flatter than $NdBa_2Cu_3O_{7-\delta}$ films?," Appl. Phys. Lett. **79**, (2001) 3660.

11. F. Giovannelli, M. Ferretti, J. F. Bardeau, M. Hervieu1 and I. Monot-Laffez, "Structural investigation of solid solution in $Nd_{1+x}Ba_{2-x}Cu_3O_{y,}$" Supercond. Sci. Technol. **17** (2004) 8.

12. J. Kramer, S. I. Yoo, R. W. McCallum, W. B. Yelon, H. Xie and P. Allenspach, "Hole filling, charge transfer and superconductivity in $Nd_{1+x}Ba_{2-x}Cu_3O_{7-\delta}$," Physica C **219** (1994) 145.

13. H. Nozaki, S. Yakekawa and Y. Ishizawa, "Superconductivity of the system $Nd_{1+2x}Ba_{2(1-x)}Cu_3O_y(0<x<0.4)$:Effect of the Magnetic Nd^{3+} Ion occupying Ba site," Jpn. J. Appl. Phy., **27** (1988) L31.

14. K. Takita, H. Katoh, H. Akinaga, M. Nishino, T. Ishigaki and H. Akinaga, " X-ray diffraction study on the crystal structure of $Nd_{1+x}Ba_{2-x}Cu_3O_{7-\delta}$" Japanese journal of applied physics, **27**, (1988) L57.

15. M. Salluzzo, C. Aruta, G. Ausanio, S. Bal, A. D. Agostino and M. G. Maglione, "Role of Nd/Ba Substitution on the growth mode and on the structural properties of Nd-rich $Re_1(Nd_xBa_{2-x})Cu3O_{7-\delta}$ (Re=Nd, Y) thin films," Physica C, **372-376** (2002) 675.

16. M. Salluzzo, I. Maggio-Aprile and O. Fisher, "Properties of superconducting $Nd_{1+x}Ba_{2-x}Cu_3O_{7-}\delta$ thin films deposited by dc magnetron sputtering," Applied physics letter, **73** (1998) 683.

17. M. Salluzzo, C. Aruta, I. Maggio-Aprile, O. Fischer, S. Bals, and J. Zegenhagen , "Growth of $R_{1+x}Ba_{2-x}Cu_3O_{7-\delta}$ epitaxial films investigated by in situ scanning tunneling microscopy," Phys. Stat. sol. (a), **186**, (2001) 339.

18. Z. Mori, T. Inoue, N. Yokoyama, S. Koba, T. Doi, Y. Hakuraku, "Effect of Nd-Ba Substitution in sputter deposited Nd_{1+x} $Ba_{2-x}Cu_3O$ (NBCO) thin film," Physica B, **284-288** (2000) 1037.

19. J. S. Bae, In-Sang Yang, W. Jo, S. H. Wee and S. I. Yoo, "Optimization of $Nd_{1+x}Ba_{2-x}Cu_3O_7$ thin film growth conditions using micro-Raman spectroscopy," Supercond. Sci. Technol., **19** (2006) 102.

20. M. Badaye, J. G. Wen, K. Fukushima, N. Koshizuka, "Superior properties of $NdBa2Cu3O_y$ over YBa2Cu3Ox thin films M Badaye et al Supercond. Sci. Technol., **10** (1997) 825.

21. A. Eulenburg, E.J. Romans, Y.C. Fan, C.M. Pegrum, "Pulse laser deposition of $YBa_2Cu_3O_{7-\delta}$ and $NdBa_2Cu_3O_{7-\delta}$ thin films: a comparative study," Physica C, **312** (1999) 91.

22. M. Badaye, F. Wang, Y. Kanke, K. Fukushima,and T. Morishita, " High quality c-axis oriented superconducting Nd1+xBa2-xCu3O7-delta thin films deposited by the laser ablation method," Appl.Phys.Lett., **66** (1995) 2131.

23. M. Badaye, W. Ting, K. Fukushima, N. Koshizuka, T. Morishita, and S. Tanaka, "Scanning probe microscopy of NdBa2Cu3Ox thin film surfaces," Appl. Phys. Lett., **67** (1995) 2155.

24. Wu Ting, N. Koshizuka and S. Tanaka, "The effect of increased humidity in air on the surface properties of c-axis oriented $Nd_1Ba_2Cu_3O_y$ thin films," Applied superconductivity, **4** (1996) 349-356.

25. G. J. Gerritsma, M. A. J. Verhoeven, R. Moerman, D. H. A. Blank, H. Rogalla, "Tunnelling barriers for high temperature superconductor devices," Journal of Alloys and Ctm,pounds, **251** (1997) 196.

26. K. Char, L. Antognazza, and T. H. Geballe, "Study of interface resistance in epitaxial $YBa_2Cu_3O_{7-x}$ /barrier/ $YBa_2Cu_3O_{7-x}$," Appl. Phys. Iett., **63**, (1993) 2420.

27. M. A. J. Verhoeven, R. Moerman, M. E. Bijlsma, A. J. H. M. Rijnders, D. H. A. Blank, G. J. Gerritsma, and H. Rogalla, " Nucleation and growth of $PrBa_2Cu_3O_{7-\delta}$ barrier layers on ramps in $DyBa_2Cu_3O_{7-\delta}$ studied by atomic force microscopy," Appl. Phys. Lett., **68** (1996) 1276.

28. D. H. Blank, G. J. H. M. Rijnders, R. M. H. Bergs, M. A. J. Verhoeven and H. Rogalla, "Characterization of ramp-type $YBa_2Cu_3O_7$ junction by AFM," IEEE Trans. Appl. Supercon., **7** (1997) 3323.

29. C. Horstmann, R. Gerber, J. L. Jia, U. Hartmann, “Influence of ramp shap and morphology on the properties of YBa2Cu3O7-δ ramp type junctions,” Physica C, **302** (1998) 176.

30. M. A. J. Verhoeven, G. J. Gerritsma, A. A. Golubov and H. Rogalla, “Ramp-type junction parameter control by Ga doping of $PrBa_2Cu_3O_{7-\delta}$ barriers,” Appl. Phys. Lett., **69** (1996) 849.

31. A. A. Golubov, M. A. J. Verhoeven, I. A. Devyatov, M. Yu. Kupriyanov, G. J. Gerritsma, and H. Rogalla, “Resonant Tunneling in $Y(Dy)Ba_2Cu_30_{7-\delta}$ / $PrBa_2Cu_{3-x}GaxO_{7-\delta}$ / $Y(Dy)Ba_2Cu_30_{7-\delta}$ Ramp- Type Josephson Junctions,” Physica *C*, **235-240** (1994) 3261.

32. A. W. Kleinsasser, “Excess currents and voltages in superconducting junctions,” Appl. Phys. Lett., **62** (1993) 193.

33. Henk-Jan H. Smilde, Hans Hilgenkamp, Guus Rijnders, Horst Rogalla, and Dave H. A. Blank, “Enhanced transparency ramp-type Josephson contacts through interlayer deposition,” Appl. Phys. Lett., **80** (2002) 4579.

34. W. H. Chang, “Measurement and calculation of Josephson junction device inductance,” J. Appl. Phys., **50** (1979) 8129.

Chapter 3

RSFQ logic circuit design

3.1 Introduction

The RSFQ concept has already been introduced in section 1.4. RSFQ logic circuits consist of a number of superconducting loops connected together in many ways to perform a desired logic function. Each superconducting loop has one or more overdamped junctions. The value of the inductance of the loop and the critical current of the junctions in the loop determine the number of stable states of the loop. The presence or absence of a magnetic flux quantum in a loop is represented by the entrance or the exit of a single flux quantum pulse across the junction by the rotation of its phase by 2π under suitable bias conditions.

In the RCSJ model, the Josephson dynamics is equivalent to an LCR oscillator with the following time constants

$$\tau_1 = RC\,, \tag{3.1}$$

$$\tau_2 = \frac{L_J}{R} \text{ where } L_J = \frac{\Phi_0}{2\pi I_C}, \tag{3.2}$$

$$\tau_0 = \sqrt{\tau_1 \tau_2}\,. \tag{3.3}$$

The damping parameter β_C is written as

$$\beta_C = \frac{\tau_1^{\,2}}{\tau_0^{\,2}} = \frac{\tau_1}{\tau_2}. \tag{3.4}$$

For an overdamped junction, the switching time is approximately given by τ_2. It is known that each data bit in the RSFQ logic is associated with an SFQ voltage pulse of quantized area of size $\int V dt = \Phi_0$. The energy associated with an SFQ pulse for a junction with a critical current of 200 μA is approximately 4×10^{-19} Joules. For an $I_C R_N$ product of 500 μV, the width of an SFQ pulse is about 2 picoseconds. The high switching speed and low power dissipation make the Josephson junction a way to achieve ultra-fast digital electronic circuits.

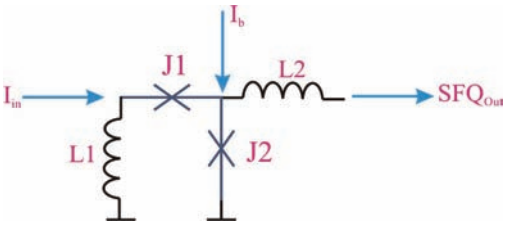


Figure 3.1: DC-SFQ converter.

A simple DC-SFQ converter, whose frequency of pulse generation is controlled by an external clock, is shown in figure 3.1. The converter consists of an asymmetrically biased dc SQUID with two current inputs, one for biasing the SQUID I_b and the other for

the clock input I_{in}. A large part of bias current I_b is flowing through junction J2. Consider a sinusoidal clock input. When I_{in} is increased to a sufficient value, junction J2 makes a 2π phase shift, generating an SFQ output, as the current contributed by both inputs added together along J2 exceeds the critical current of J2. Now, the bias current I_b is diverted along J1. When I_{in} is decreased below a certain value, the bias current will make J1 to switch to restore the initial state of the SQUID loop. By choosing proper bias conditions, for every clock period, an SFQ pulse can be generated at the output junction J2.

3.2 Transmission and storage of SFQ pulses

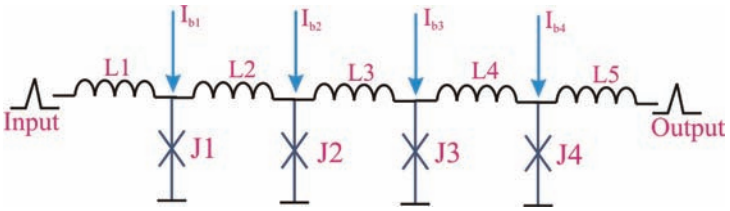


Figure 3.2: Josephson transmission line.

An array of identical junctions connected in parallel by superconducting inductors forms a Josephson Transmission Line (JTL) as shown in figure 3.2. Each junction is biased by a current lower than its critical current. For $LI_C < \Phi_0$, an SFQ pulse generated by junction J1 is reproduced by junction J4 by successive switching of junctions J2 and J3. A JTL can also be used to amplify SFQ pulses [1].

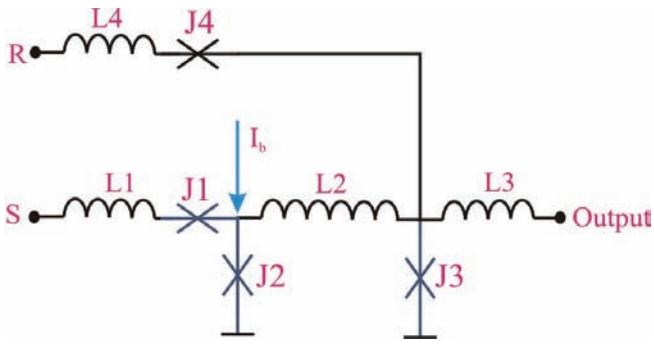


Figure 3.3: RS flip-flop.

Consider two identical junctions forming a DC SQUID with an inductance L. For $LI_C = 1.5\Phi_0$, the SQUID has two stable states, storing either zero or one fluxon. A memory element, called an RS flip-flop works according to this principle. An RS flip-flop is shown in figure 3.3. The loop with junctions J1 and J3 is the memory element in this circuit. Initially, when there is no fluxon in the memory element, most of the bias current I_b is flowing through junction J2. Now, a triggering pulse (or an SFQ pulse) applied at the point S induces a 2π rotation of the phase of the Josephson junction. This corresponds to an SFQ pulse across junction J2 and a fluxon enters the loop. The fluxon

will be stored in the loop until a pulse is applied at terminal R to switch junction J3. Now, the stored fluxon escapes through junction J3 to let the state of the loop return to its initial stage. Buffer junctions J1 and J4 prevent the change of the state of the loop by false input pulses [1].

3.3 Superconducting passive transmission line

Josephson transmission lines are normally used for transmitting pulses between RSFQ circuits. But connecting RSFQ circuits over long distances using a JTL, introduces a large propagation delay time. One can use superconducting passive transmission lines instead to obtain high speed SFQ pulse transmission.

Figure 3.4 shows the cross section of a superconducting transmission line.

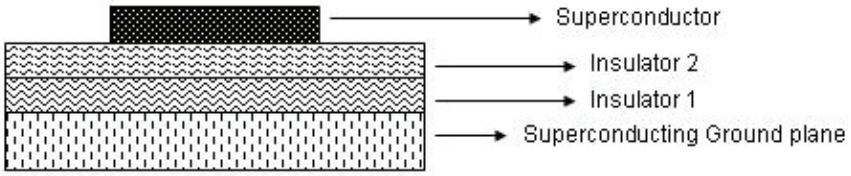


Figure 3.4: Cross section of a superconducting micro-strip line.

The characteristic impedance of the transmission line is given by

$$Z_0 = \sqrt{\frac{L}{C}}\,. \tag{3.5}$$

L is the inductance per unit length and C is the capacitance per unit length of the transmission line.

$$L = \frac{\mu_0}{kW}\left[t_{in1} + t_{in2} + \lambda_1 \coth\left(\frac{t_1}{\lambda_1}\right) + \lambda_2 \coth\left(\frac{t_2}{\lambda_2}\right)\right], \tag{3.6}$$

$$C = \frac{k\varepsilon_0 W}{\left[\frac{t_{in1}}{\varepsilon_1} + \frac{t_{in2}}{\varepsilon_2}\right]}, \tag{3.7}$$

where W is the width of the top superconducting film. λ_1 and λ_2 are the penetration depth of the ground plane and the top superconducting film. t_1 and t_2 are the thickness of the ground plane and the top superconducting film. t_{in1} and t_{in2} are the thicknesses of the insulation layers. ε_1 and ε_2 are the dielectric constants of the insulating layers, μ_0 is the permeability of free space and k is the fringing factor.

Impedance matching is necessary between a JTL and the passive line in order to prevent undesirable reflection [2]. There are reports by some groups simulating and testing SFQ circuits with passive transmission lines for pulse propagation [13-15]. From the simulation it was found that the operating margin is large for a perfectly matched passive transmission line and receiver. The impedance of a JTL is given by

$$Z_{JTL} = \frac{L_{JTL}}{\tau_{JTL}}, \tag{3.8}$$

where L_{JTL} and τ_{JTL} are the inductance and the propagation delay time of a JTL stage respectively [3]. The impedance can also be calculated by the following relation,

$$Z_{JTL} = \left(\frac{I_B}{I_C}\right) R_N, \tag{3.9}$$

where I_B, I_c and R_n are the bias current, critical current and normal state resistance of the Josephson junction [13]. Flux trapping is avoided by introducing a series resister at the end of the passive transmission line.

3.4 Effect of temperature

According to the RCSJ model, a current biased and fluctuation free Josephson junction is represented by the following equation.

$$\mathrm{M}\frac{d^2\phi}{dt^2} + \frac{\mathrm{M}}{RC}\frac{d\phi}{dt} + \frac{\partial U(\phi)}{\partial \phi} = 0. \tag{3.10}$$

This is equivalent to the motion of a particle of mass $\mathrm{M} = C(\Phi_0/2\pi)^2$ in a washboard potential $U(\phi)$. The potential, $U(\phi)$ is given by

$$U(\phi) = -E_J\left(\frac{I}{I_C}\phi + \cos\phi\right). \tag{3.11}$$

The slope of the potential is proportional to the applied current *I*. For $I<I_C$, the particle is localized in one of the potential wells at zero temperature. This situation corresponds to the zero voltage state of the junction. At finite temperature, the particle can escape from the potential well under the influence of thermal fluctuations depending on the height of the barrier. The Josephson coupling energy has to be much higher than the thermal energy to avoid false switching by thermal noise, i.e.

$$\frac{\Phi_0 I_C}{2\pi} >> k_B T. \tag{3.12}$$

On the basis of a thermal activation model, it was shown that [4]

$$\frac{\Phi_0 I_C}{2\pi k_B T} \approx 60. \tag{3.13}$$

At a finite temperature, different switching errors happen in the HTS devices. A stored flux quantum in a memory element can escape by false switching of the junction due to thermal noise, which is called storage error or static error [5]. Thermal fluctuations cause an uncertainty in the arrival time of the data pulse (pulse jitter) [6]. This happens for high speed circuits in which there is an interaction between the pulses. In a two junction comparator [7], when the input current is near the threshold value, the wrong junction can switch upon the application of the sampling clock pulse [8]. Ruck *et al.* reported that HTS RSFQ circuits can be operated up to 40K with a reasonable Bit Error Rate (BER) and circuit parameter margins [9].

When the width of the junction is longer than the Josephson penetration depth λ_J, the self-field effect is dominant and the junction shows flux flow behavior [10]. The junction width should be less than $4\lambda_J$ to avoid this effect.

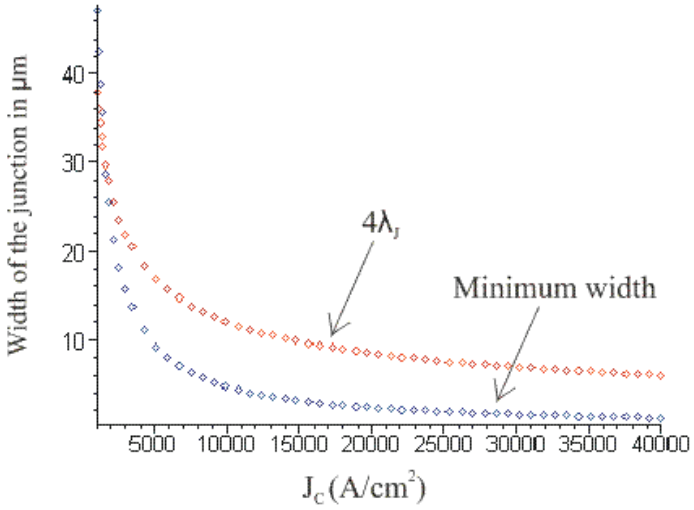


Figure 3.5: A plot of the junction width versus current density at 30 K.

The minimum width of the junction is derived by using equation (3.13),

$$\text{Minimum junction width} = \frac{120\pi k_B T}{\Phi_0 J_c t}. \tag{3.14}$$

The range of junction widths between the long junction limit and the minimum width defined by the thermal fluctuation for different values of Josephson current density is shown in figure 3.5 at 30 K.

3.5 Mask design

Special software tools (circuit simulators, layout editors, inductance estimators, optimizers) are necessary for the design of RSFQ circuits. To speed up designing complex circuits, an integrated environment to exchange data between the different tools is needed. A flow chart describing the design process is shown in figure 3.6.

The circuit description has to be defined clearly. A netlist can be generated manually depending on the circuit simulator used. Some simulators have their own schematic editor like in WINS [11]. Depending on the HTS junction technology, the $I_C R_N$ product and β_C values are fixed before the simulation. The circuit is simulated repeatedly by changing the input parameters until a correct operation is obtained. Once we have a set of parameters for the correct operation, the optimum values of the parameter (critical currents, inductances, bias currents and resistances) can be found by using optimization tools. We used XOPT [12] for our design. XOPT uses design centering methods to obtain circuit parameters with the highest margins to have a maximum fabrication yield.

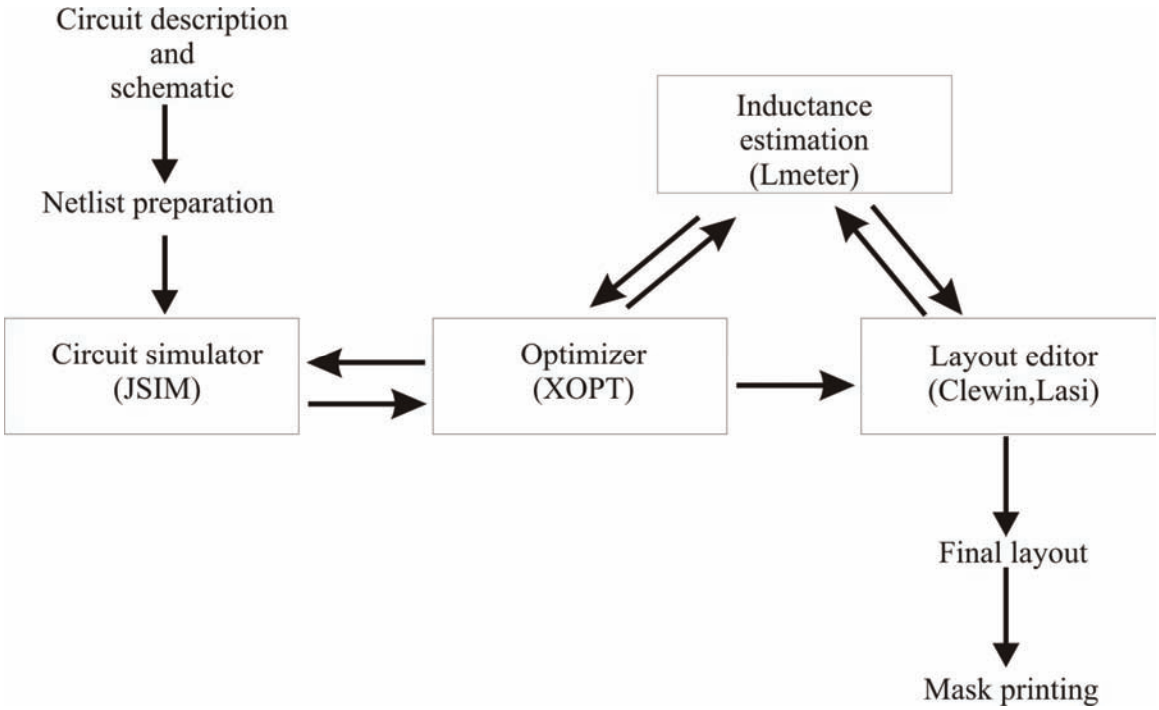


Figure 3.6: Design flow diagram for RSFQ circuit design.

The layout of the circuit is drawn using the parameters finally obtained from the optimizer. An inductance estimator extracts inductances from the mask layout supplied by the layout editor. Design rules such as minimum layer width, overlapping length between two layers, minimum distance between the strip lines and critical current density have to be defined during the layout design. Constraints imposed by the design rules may introduce unavoidable parasitic inductances in the circuit layout. A correct operation of the circuit has to be verified if any additional parasitic elements are added. Once we have a final layout, the mask is printed.

Cell-based design is used for the integrated circuits. Standard cells are designed for repeatedly used circuit elements. Interaction between the cells should be very low to increase the circuit margins. Some frequently used cells, optimized for a maximum yield are given in appendix 1.

3.6 Conclusion

RSFQ logic circuits use SFQ pulses, generated by Josephson junctions, to send and store digital information. RSFQ circuits can operate at high frequencies, beyond, 100 GHz, dissipating a very low power of the order of 10^{-18} joule per bit. The low power consumption increases the circuit density and reduces the propagation delay between the circuit elements.

Passive transmission lines are used to transfer SFQ data to distant RSFQ circuits with high speed, approaching that of light. There is no attenuation and dispersion of SFQ pulses passing over a distance of a few centimeters.

Thermal fluctuations can make a junction to switch spontaneously and introduce errors in circuit function. Fluctuations introduce timing delays and increase the chance of switching the wrong junction.

The procedures involved in the mask production (the design of the RSFQ circuits, optimization of the parameters to have a maximum fabrication yield, layout editing and inductance extraction) have been discussed. Parasitic inductances, introduced due to the design rules, require re-optimization of circuits.

References

1. K. K. Likharev and V. K. Semenov, “RSFQ logic/ Memory family: a new Josephson junction technology for sub-terahertz clock frequency digital systems,” IEEE. Trans. Appl. Supercond., **1** (1991) 3.

2. Z. John Deng, N. Yoshikawa, S. R. Whiteley and Theodore Van Duzer, “Self-Timing and Vector Processing in RSFQ Digital Circuit Technology,” IEEE Trans. Appl. Supercond., **9** (1999) 7.

3. S. V. Polonsky, V. K. Semenov, and D. F. Schneider, “Transmission of single-flux-quantum along superconducting microstrip lines,” IEEE Trans. Appl. Supercond., **3** (1993) 2598.

4. H. Tofer, T. Ortlepp, H. F. Uhlmann, D.Cassel, and M. Siegel, “Design of HTS RSFQ circuits,” Physica C, 392-396 (2003) 1420.

5. A. V. Rylyakov, K. K. Likharev, “Pulse jitter and timing errors in RSFO circuits,” IEEE Trans. Appl. Supercond. **9** (1999) 3539.

6. V. Kaplunenko and V. Borzenets, “Timing Jitter measurement in a circular Josephson transmission line,” IEEE Trans. Appl. Supercond., **11** (2001) 288.

7. T. V. Fllippov, and V. K. Kornev, “ sensitivity of a Josephson junction comparator,” IEEE Trans. Magnetics, **27** (1991) 2452.

8. Q. P. Herr and M. J. Feldman “Error rate of a superconducting circuit,” Appl. Phys. Lett., **69** (1996) 694.

9. B. Ruck, B. Oelze, R. Dittmann, A. Engelhardt, E. Sodtke, W. E. Booij and M. G. Blamire, “Measurement of the dynamic error rate of a high temperature

superconductor rapid single flux quantum comparator," Applied Physics Letters, **72** (1998) 2328.

10. T. Van Duzer and C. Turner,"Principles of Superconductive Devices and Circuits" Prentice Hall, 1999.

11. http://www.kapl.tv/wins_text.htm

12. T. Harnisch, J.Kunert, J. Toepfer, and H. F. Uhlmann, "Design centering methods for yield optimization of cryoelectronics circuits," IEEE Trans. Appl. Supercond., **7** (1997) 3434.

13. H. Suzuki, S. Nagasawa, H. Hasegawa, T. Hashimoto, K. Miyahara, and Y. Enomoto, "High frequency operation of JTL ring oscillator with a passive transmission line," IEEE Trans. Appl. Supercond., **11** (2001) 1082.

14. Z. J. Deng, N. Yoshikawa, S. R. Whiteley, and T. Van Duzer, "Self-Timing and Vector Processing in RSFQ Digital Circuit Technology," IEEE Trans. Appl. Supercond., **9** (1999) 7.

15. D. Gupta and Y. Shang, "On-chip clock technology for ultrafast digital superconducting electronics," Physics Letters, **76** (2000) 3819.

Chapter 4

A/D converter in Josephson technology

4.1 Introduction

In communication systems (mobile telephony, GPS systems and internet) AD converters with 12-16 bit resolution and linearity are necessary [1]. In medicine, a sensitive instrument like ECG (electrocardiogram) requires 24 bit resolution at low frequencies [2]. Delta-Sigma modulators can achieve a medium to high resolution for a wide signal bandwidth suitable for wireless communication. A high resolution is obtained by using over-sampling and noise shaping. Over-sampling reduces the quantization noise power within the signal band width. Noise shaping pushes most of the in-band noise outside the signal bandwidth by using a feedback arrangement and digital filtering. It is simple to implement this modulator as it uses a single bit quantizer. Oversampling requires a high speed and complex digital signal processing unit [3]. Josephson junctions enable GHz sampling for a MHz signal bandwidth providing a high dynamic range.

A block diagram of a first order delta-sigma modulator is shown in figure 4.1. The modulator consists of an integrator, quantizer and a feedback loop. The integral of the difference between the input (X) and the quantized output (Y) is fed to the quantizer. The average value of the quantized output is forced to be equal to the input signal by the closed loop feedback system [3].

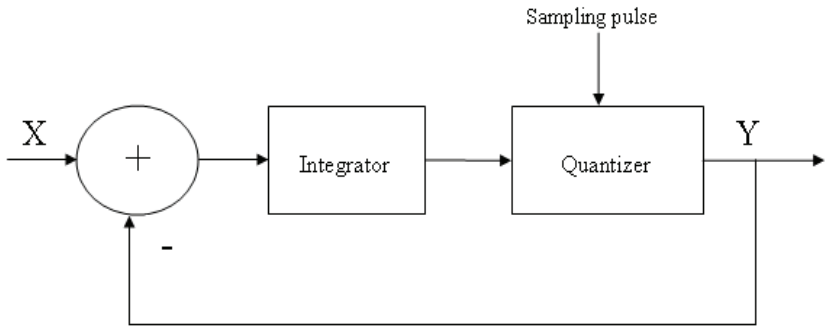


Figure 4.1: A block diagram of a first order delta-sigma modulator.

The SNR (Signal to Noise Ratio) of a first order delta-sigma modulator is given by

$$SNR = 10\log\left(\frac{3}{2}2^{2N}\right) + 10\log\left(\frac{3}{\pi^2}(OSR)^3\right), \tag{4.1}$$

where N is the number of bits and OSR is the oversampling ratio given by the sampling frequency divided by two times the signal frequency. Each doubling of the sampling frequency increases the SNR by 9 dB or 1.5 bits.

4.2 Higher order modulator

In the first order delta-sigma modulator, the OSR should be greater than 1500 to get 16 bit resolution. By adding additional feedback loops, the same resolution can be obtained by further suppression of noise in the signal band with lower OSR. Consider a second order modulator as shown in figure 4.2.

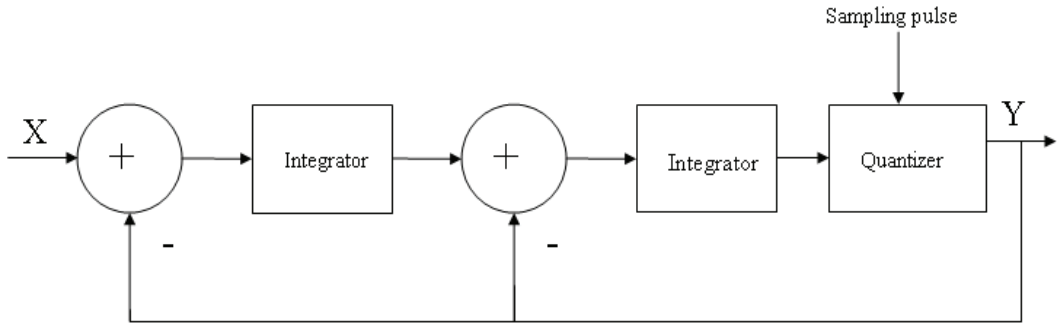


Figure 4.2: A block diagram of a second order delta-sigma modulator.

The modulator has two integrators and two feed back loops. The SNR value is given by

$$SNR = 10\log\left(\frac{3}{2}2^{2N}\right) + 10\log\left(\frac{5}{\pi^4}(OSR)^5\right). \tag{4.2}$$

Here, the SNR increases by 15 dB or 2.5 bits for every doubling of the OSR. In general, for L loops, every doubling of the OSR provides $(L+0.5)$ extra bits [3]. In general, higher order modulators (L>2) suffer from stability problems and complexity in design. So there are always tradeoffs between resolution, bandwidth, circuit complexity and stability of the modulators, when higher order delta-sigma modulators are considered [4].

4.3. Delta-sigma modulator in Josephson technology

A first order Josephson delta-sigma modulator is shown in figure 4.3.

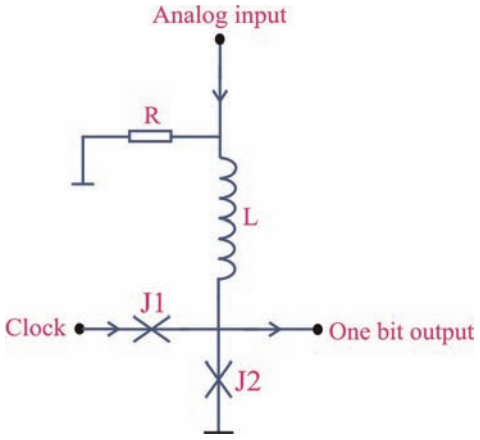


Figure 4.3: Superconducting first order delta-sigma modulator.

The integrator is a simple RL network. An analog signal is applied to the Josephson comparator through the integrator [5]. Clock pulses are generated by the DC-SFQ generator and applied to the comparator via a JTL and the buffer junction. When the integrated current together with the clock pulse and the bias current exceeds the critical current of the quantizer junction J_2, an SFQ pulse is generated at the output and the current through the inductor is reduced by Φ_0 / L as an intrinsic feedback by the quantization principle. From a spectral analysis, the quantization noise is flat for frequencies less than $2\pi R / L$ [5]. For a better performance, the value of the inductance can be increased. The maximum value of the inductance is limited by the feedback current which should be higher than the noise current of the quantizer junction.

First order modulators have been realized both in LTS [6] and HTS [7] technology due to their simple design. As mentioned before, to improve the dynamic range at low sampling rate, higher order modulators are needed.

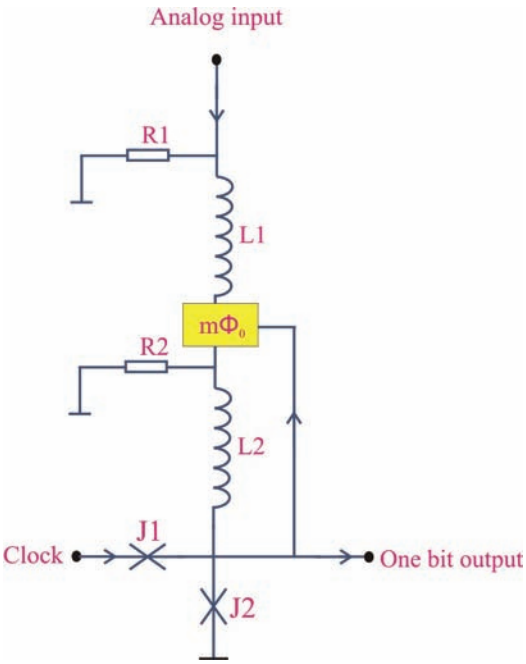


Figure 4.4: Superconducting second order delta-sigma modulator [8].

The schematic of a second order modulator is shown in figure 4.4. A signal current is applied across a resistor R_1, coupling a signal voltage to the first inductor L_1. The integrated current in L_1 is applied to another resistor R_2. The voltage across R_2 is integrated by the inductor L_2. Now, the integrated current in L_2 is sampled by the comparator junction J_2. Each SFQ output reduces the current in L_2 by (Φ_0 / L_2) and in L_1 by $(m\Phi_0 / L_1)$ due to the multi-flux quantum feedback. *m* is the number of flux quanta applied to the first integrator loop containing L_1 and R_1.

4.4 Second order modulator design

A designed second order delta-sigma modulator is shown in figure 4.5. The analog signal is integrated by two successive integrators and then sampled by the comparator circuit. The output of the comparator is fed to a splitter. One of the splitter ports is sent to a JTL and taken as output. The other port sets the RS-flip-flop comprising J6, J7 and L3. The flip-flop will be reset by a clock signal of such a frequency that the duration between the set and reset pulse is less than the time period of the sampling clock. Setting and resetting the flip-flop will change the direction of the current in the inductor L4, which is mutually coupled to L3. So the flux quantum pulses generated by the junction J8 will be transferred to J11 during the time the flip-flop is in the 'on'-state. The pulses across J11 will be applied to the first integrator via a DC isolator [15], a feed back driver and J17. The number of pulses (*m*) fed back to the first integrator, will depend on the frequency of the pulses generated across J8 and the time, for which the flip-flop is in the 'on'-state. The pulses across J11 will be applied to the first integrator via a DC isolator, a feedback driver and J17. The number *m* of feedback pulses to the first integrator will depend on the frequency of the pulses generated across J8 and the time, for which the flip-flop is in the 'on'-state. The number of feedback pulses will be controlled by carefully choosing the frequency of the clock pulse of the feedback pulse generator, and the reset pulse generator.

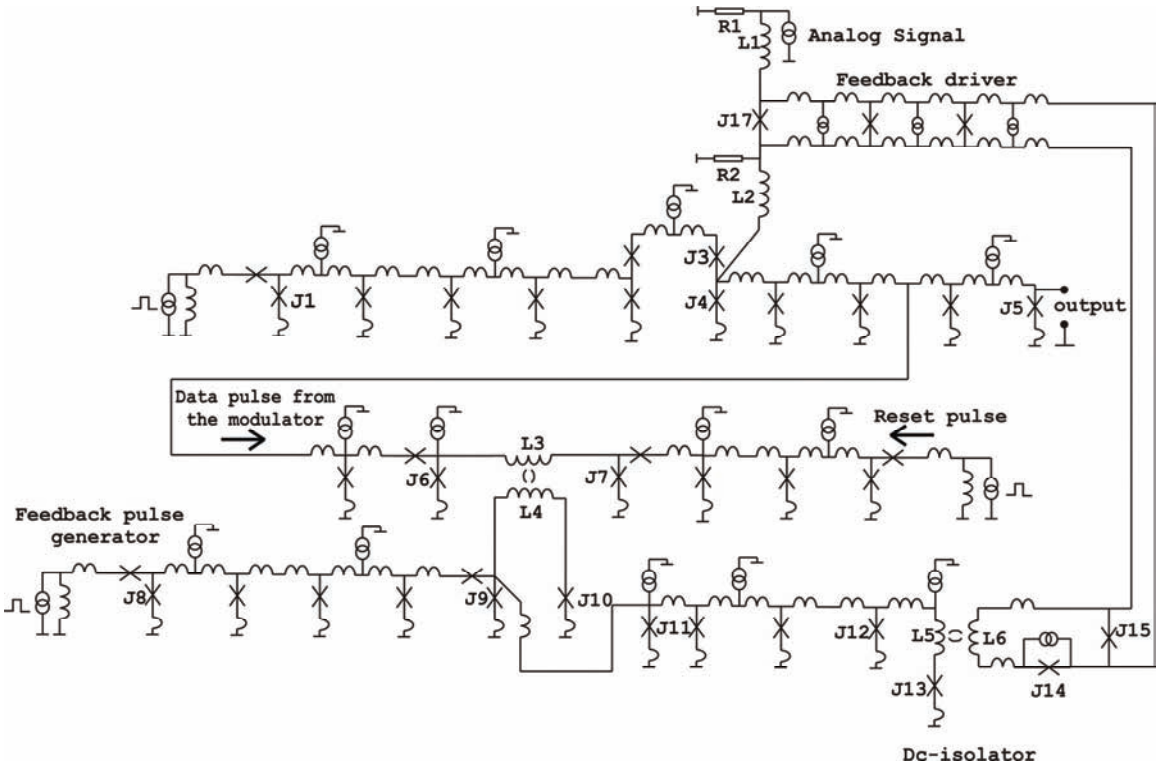


Figure 4.5: Second order modulator schematic.

4.5 Simulation results and discussion

A JSIM [12] simulation of the second order modulator for one cycle of the input signal is shown in figure 4.6. A sharp decrease in the inductor current of both integrators occurs for every modulator output within the sampling interval. The number of feedback pulses in this simulation was 5. As the value of the inductance for both integrators are the same, the inductor current of the first integrator drops 5 times more than that of the first integrator.

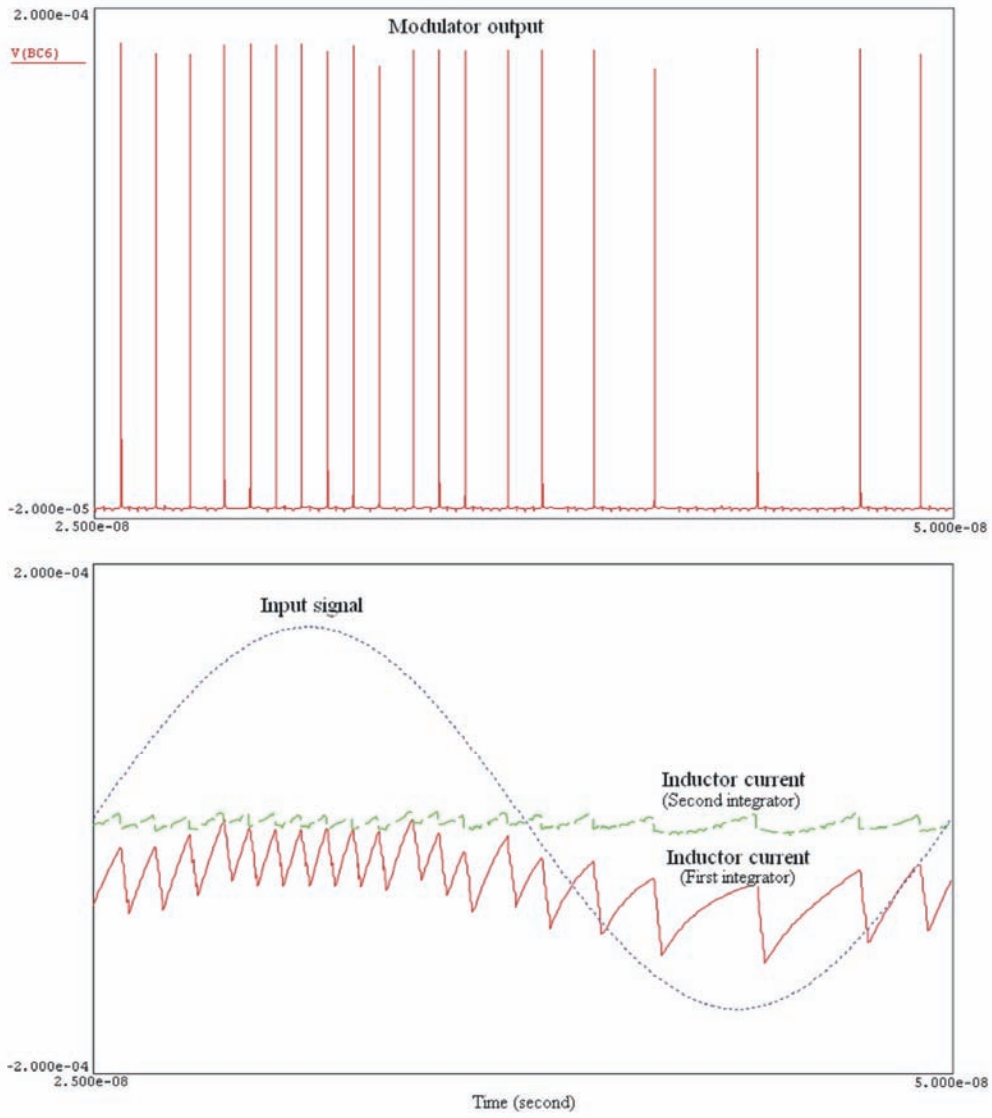


Figure 4.6: SFQ dynamics of the modulator simulated by JSIM.

To find out the dynamic range of the modulator, a Fast Fourier Transform (FFT) of the output has been taken. A JSIM simulation was carried out to take 2097152 consecutive data points with a time interval of 0.5 ps. The FFT of the modulator output is shown in figure 4.7. The Fourier spectrum shows the characteristic noise shaping

property giving a dynamic range of nearly 96 dB for a 40 MHz signal at a 10 GHz sampling rate. The broadening of power near the input signal might be connected to spectral leakage due to the non-integral number of input cycles taken to calculate the FFT.

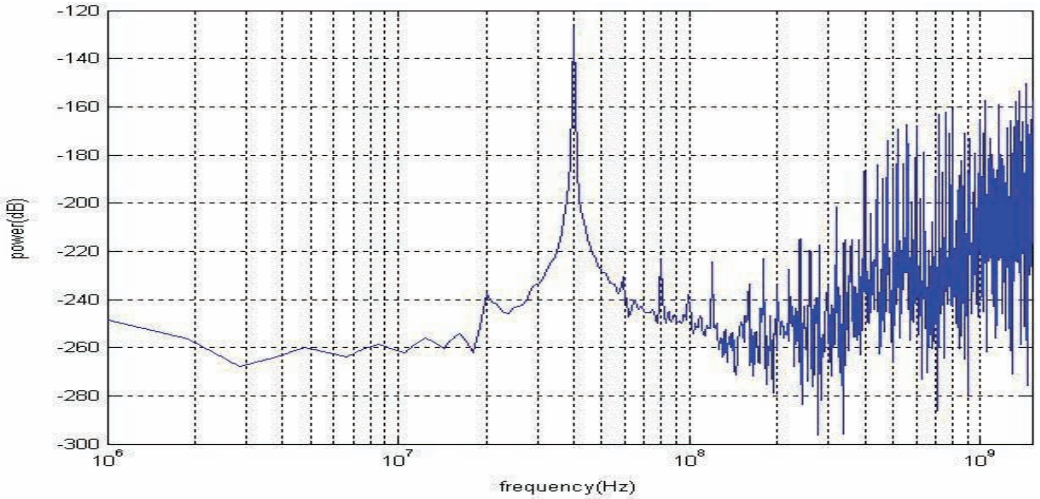


Figure 4.7: Power spectrum of the second order modulator (input frequency is 40 MHz; sampling frequency is 10GHz; feedback gain=4).

To maintain a good performance of the modulator, the number of the feedback pulses for every modulator output should be same. Let the clock period of the feed back pulse generation be denoted as t_{fb}. The time period, t_{ff} for which the flip-flop is on, is taken as the integral multiple of t_{fb}. The maximum value of t_{ff} is limited by the sampling frequency.

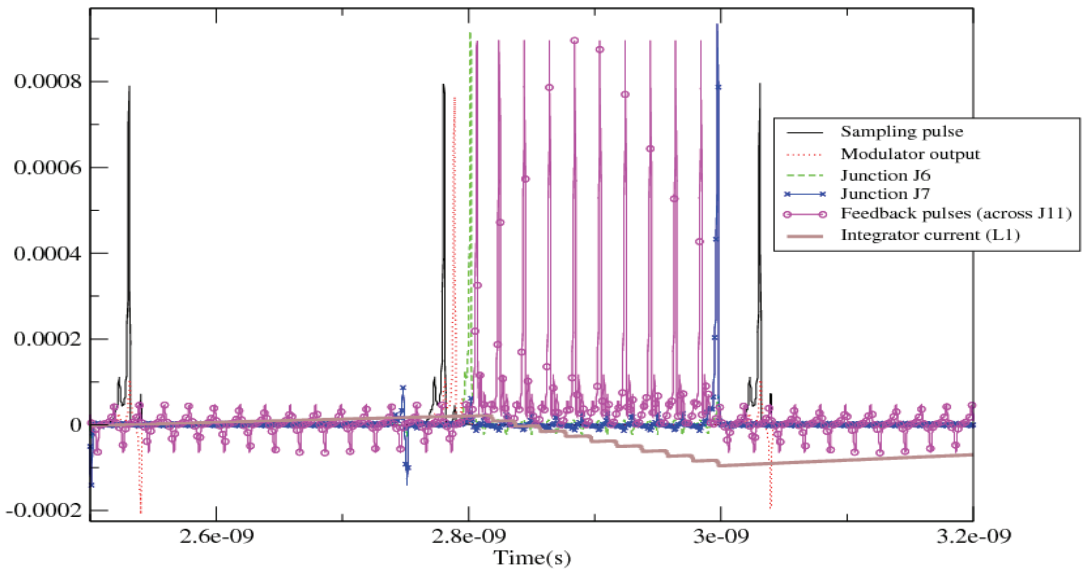


Figure 4.8: Simulation of second order modulator with 10 feedback pulses.

Figure 4.8 shows part of a simulation with a feedback gain of 10 at a sampling frequency of 4 GHz. The performance of the modulator is not affected by the arrival time of the feedback pulses within the sampling interval [13], which has been checked by making a small shift in the clock period of the feedback pulse generation. The quantization noise in the signal bandwidth is reduced further by increasing the number of feedback pulses (*m*) applied to the first integrator [14, 15]. A power spectrum of the modulator with a feedback gain of 10 is shown in figure 4.9.

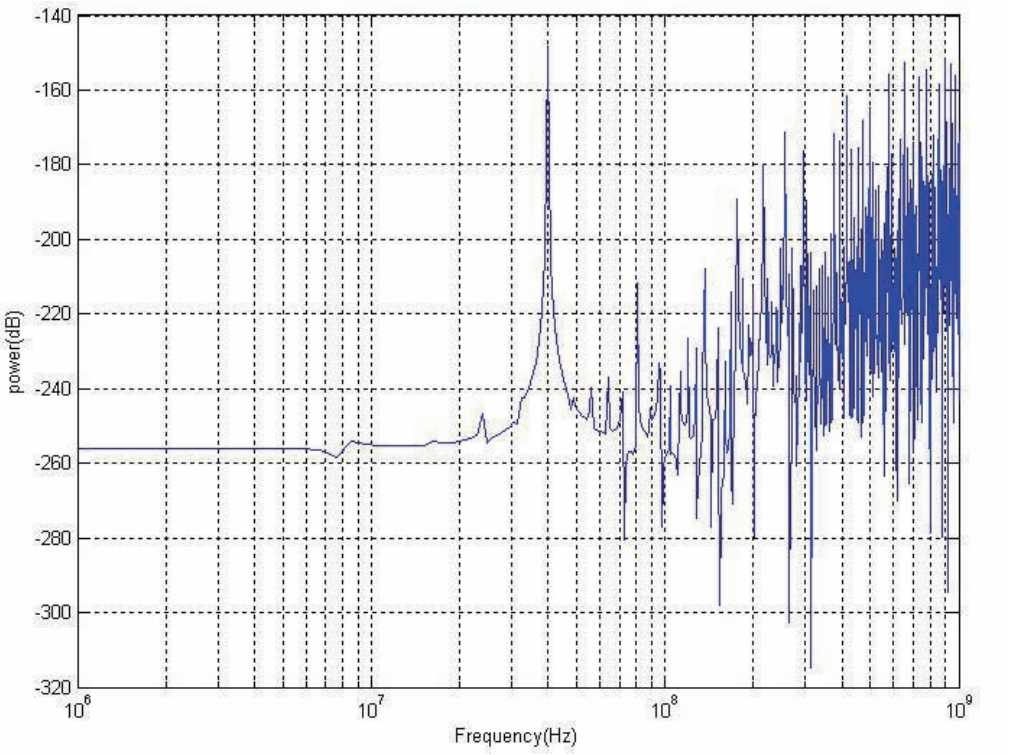


Figure 4.9: Modulator power spectrum
(Input frequency is 40 MHz; Sampling frequency is 4GHz; Feedback gain=10; L_1=L_2=150pH and R_1=R_2=.04 Ω).

A Signal to Noise Ratio (SNR) of nearly 90 dB (for a bandwidth of 75 MHz) has been obtained for a feedback gain of 10 at low OSR. As the integrator cut-off frequency is 40 MHz, the quantization noise is almost flat below 40 MHz. The appearance of spurs along with higher order harmonics, while using a current source as an input signal is suppressed strongly by increasing the L/R value. Figure 4.10 shows the modulator output power spectrum for a high L/R value.

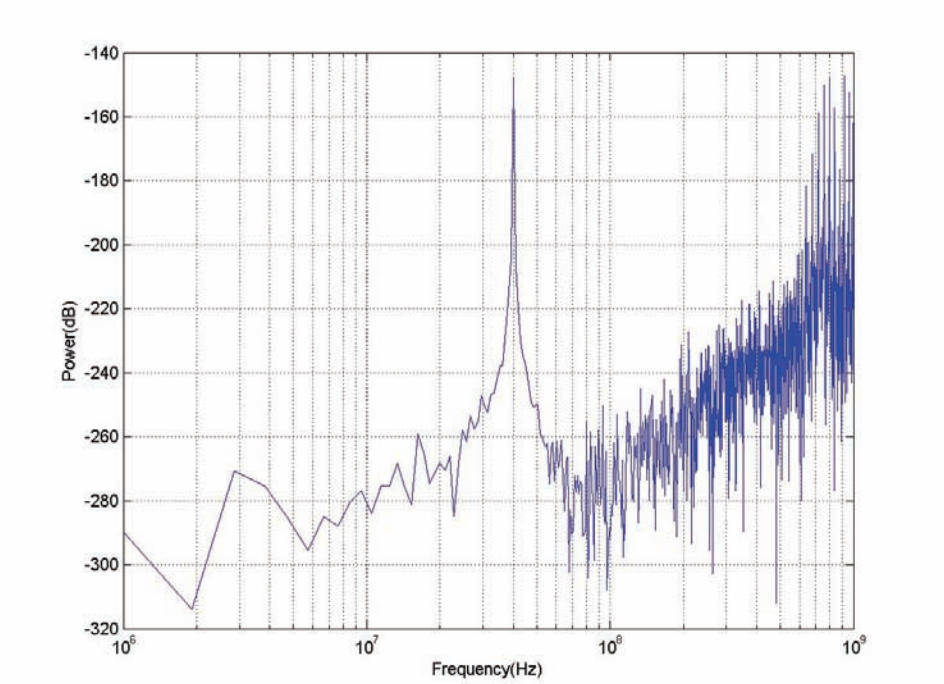


Figure 4.10: Power spectrum of the modulator. (Input frequency is 40MHz; Feedback gain = 5; sampling frequency is 10GHz; L_1=L_2=200pH and R_1=R_2=.04 Ω).

As a real input signal contains mixed frequencies, a simulation was performed by using two different input signals of the same amplitude at the first integrator. From the FFT analysis shown in figure 4.11, it was found that both signals have the same power with a SNR above 80 dB.

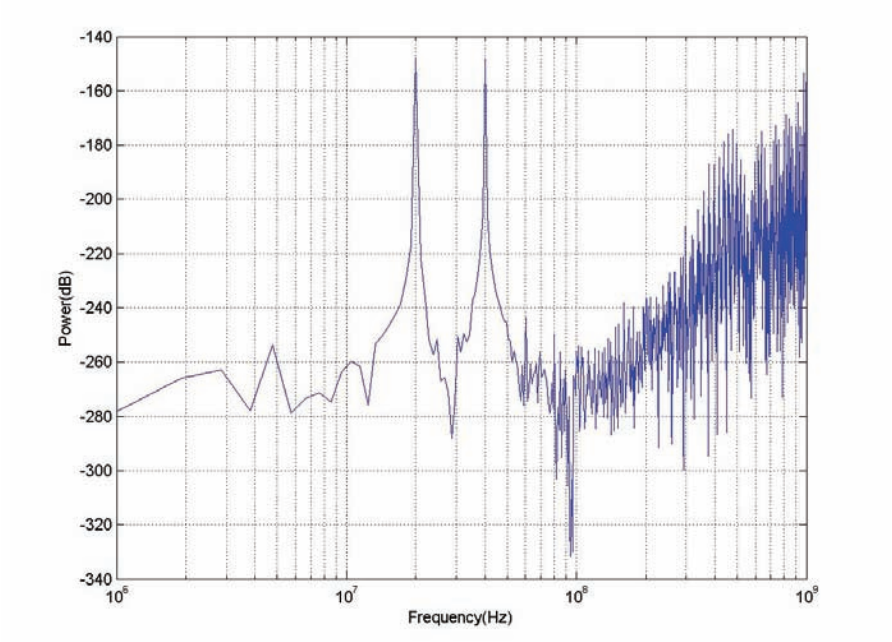


Figure 4.11: Power spectrum of the modulator with two input signal (20, 40 MHz) and M=5 at a sampling frequency of 10GHz.

4.5 Possible realization in HTS technology

In the second order delta-sigma modulator, the feedback to the second integrator (figure 4.4) is given by the quantizer junction itself at the time of sampling. The complexity of the circuit increases with the feedback loop to the first integrator (L_1 & R_1). The number of junctions in this design is 40. Therefore it is a challenging work to fabricate the whole circuit on a single chip in HTS technology unless the circuit tolerates a higher parameter spread. Since the designed circuit utilizes inductive coupling at two places, the circuit can be divided into two parts (figure 4.12) and one can fabricate each part on separate chips and they can be pressed together in a flip-chip configuration. The value of the coupling coefficient should then not be less than 0.4 (between the inductors L_3 and L_4 and between the inductors L_5 and L_6) for a good performance.

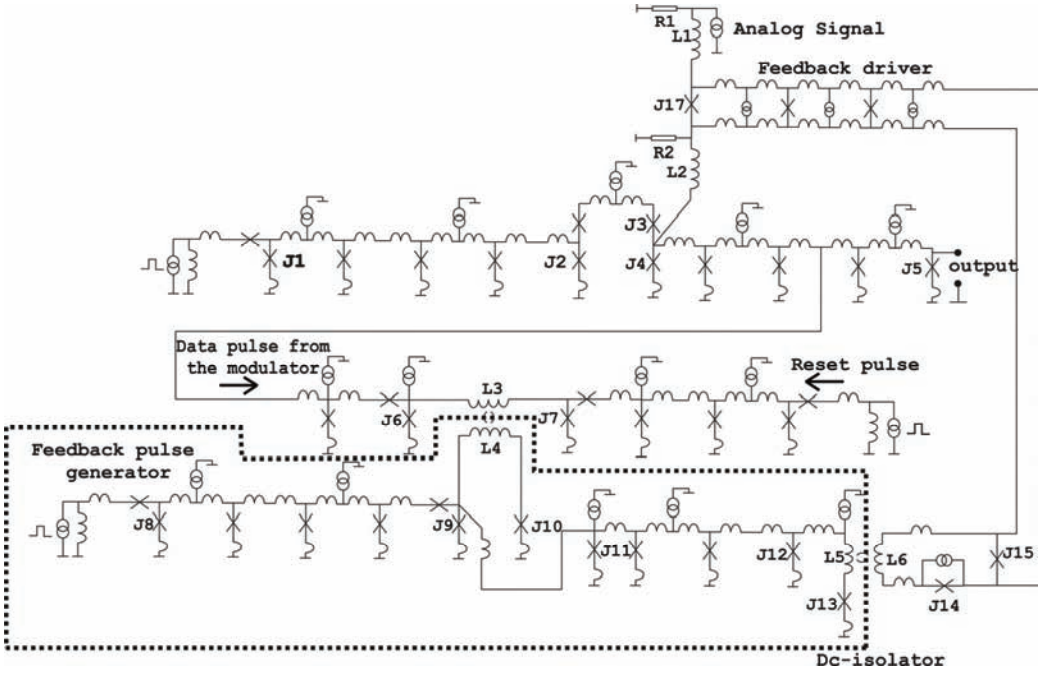


Figure 4.12: Splitting of modulator circuit into two parts which can be coupled to each other by flip-chip technology.

The performance of the modulator is mainly affected by the properties of the Josephson comparator comprising junctions J3 and J4. Due to fluctuations, both the junctions may switch simultaneously near the threshold of the comparator upon the application of the clock SFQ pulse [9]. The range of input current I_x for which the comparator shows this behavior is known as the grey zone (ΔI_x). It increases with the operating temperature and the sampling frequency [10, 11]. All the parameters of the comparator have been optimized and a set of optimized parameters are given in appendix 1.

A simulation study has been done on the fabrication yield of the DC-isolator which is one of the critical parts of the circuit. Feedback pulses are transferred to the

feedback driver by the two inductively coupled SQUID configuration under proper current biasing conditions. The circuit schematic is shown in figure 4.13.

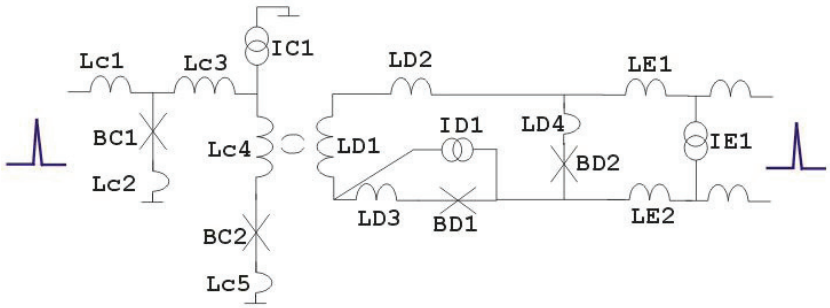


Figure 4.13: Dc-isolator schematics.

Figure 4.14 shows the margin calculation of the dc-isolator for k=0.4, where the constant k is the coupling coefficient between the inductors LC4 and LD1.

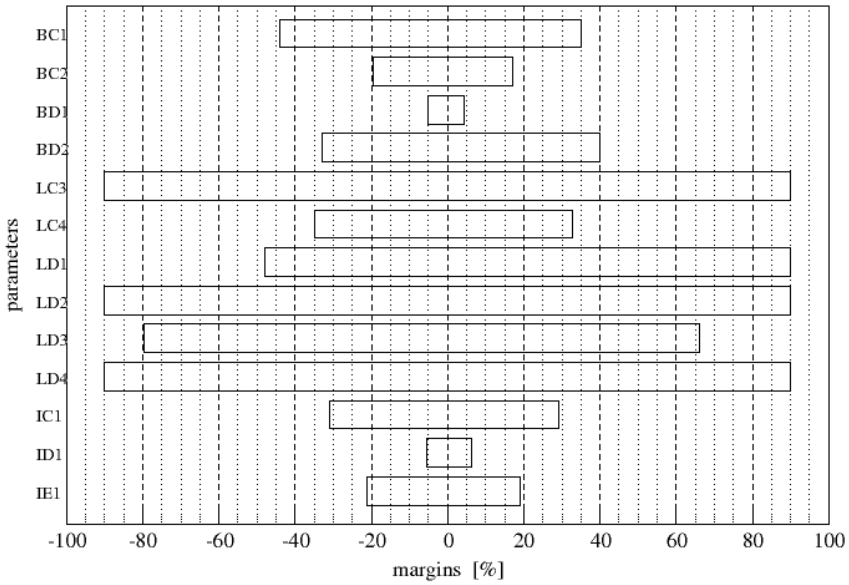


Figure 4.14: Dc-isolator margin calculation.

The critical current of junction BD1 and the bias current ID1 showed less than 10% margin in the simulation. But the spread in junction BD1 can be adjusted by changing the bias current ID1 without changing other parameters as shown in figure 4.15.

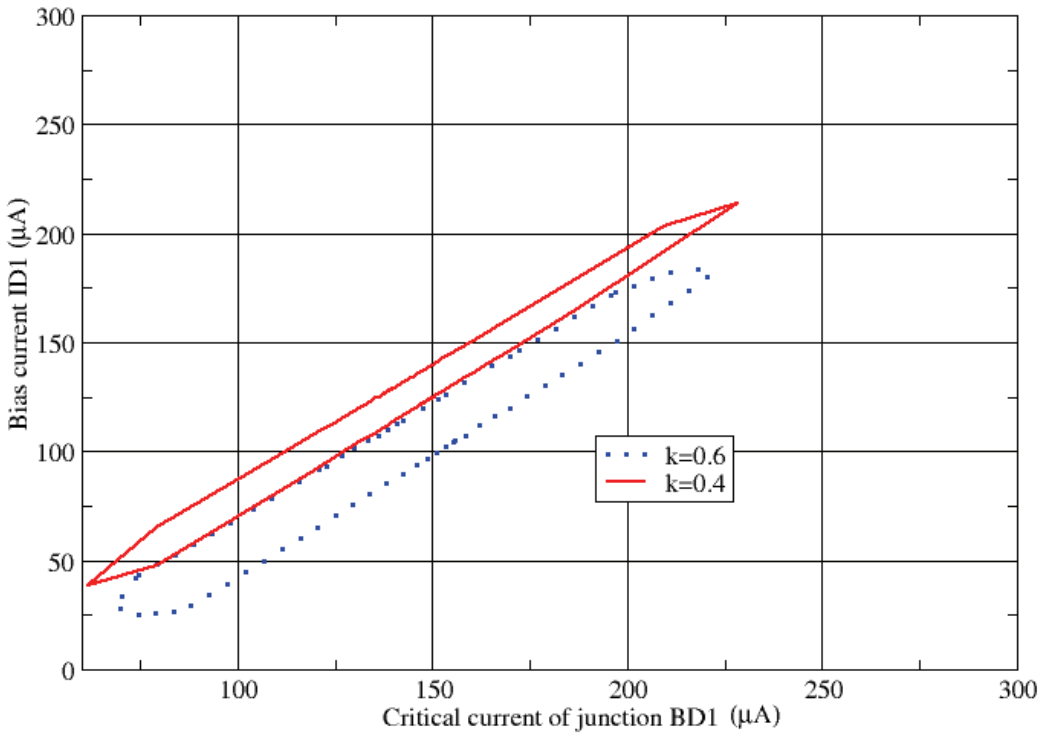


Figure 4.15: 2D margin plot of critical current of junction BD1 versus bias current ID1.

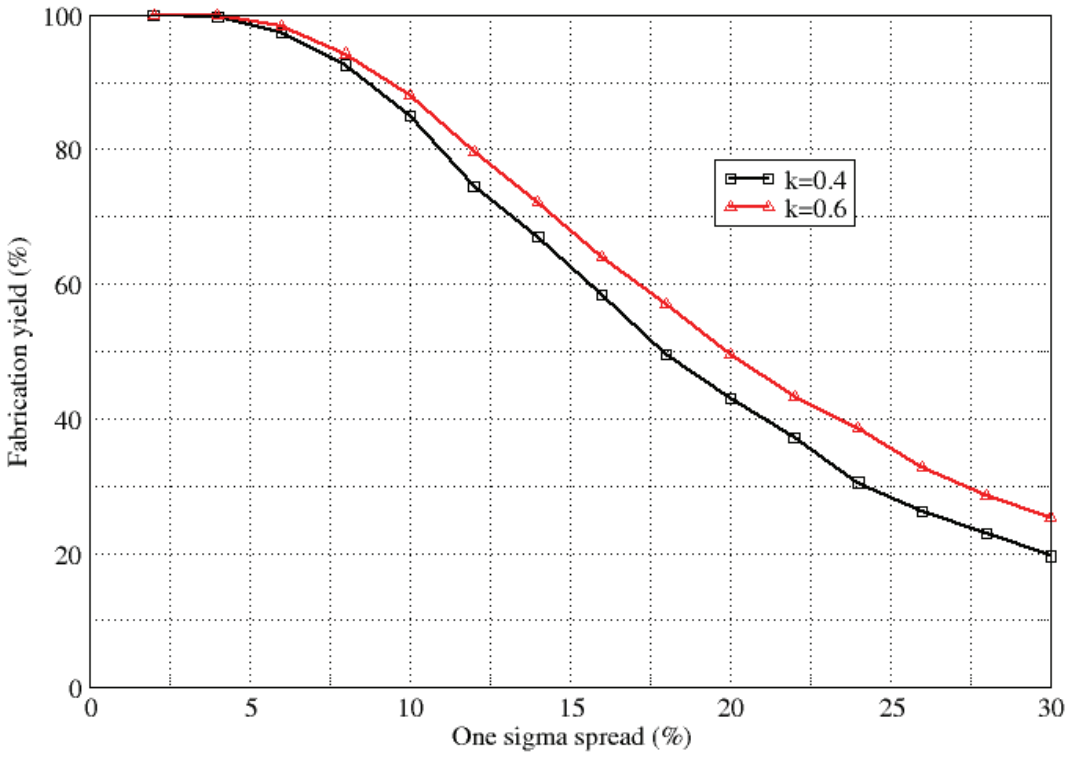


Figure 4.16: Yield calculations for different *k*.

Fabrication yield studies for different values of k were done and are shown in figure 4.16. For a 15 % spread in the technology, more than 60% fabrication yield can be obtained.

4.6 Conclusion

A superconducting second order delta-sigma modulator has been designed and simulated. Its realization in HTS technology has been discussed. The design consists of a comparator that quantizes the signal current, integrated by two integrators. The feedback to the first integrator is given by the quantizer junction. A flip-flop coupled to an inductor, together with a feedback pulse generator, decides the number of pulses fed back to the first integrator. A dc isolator and a feedback driver guide the pulses to apply feedback gain to the second integrator. The correct operation of the modulator is verified by simulation and a FFT analysis. The integrator response, the oversampling ratio and the feedback gain determine the dynamic range of the modulator.

The modulator has three DC/SFQ converters whose output frequencies can be controlled externally by stable clock generators at GHz frequencies. Two pairs of coupled inductors exist in the flip-flop element and in the dc-isolator. Simulation studies showed that a correct function of the modulator was observed for a low coupling constant of 0.4. If the parameters of the critical elements in the circuit can be controlled, one can possibly realize the second order modulator in HTS technology.

References

1. S. Yan and E. S. Sinencio, “A Continuous-Time Sigma Dleta Modulator With 88-dB Dynamic Range and 1.1-MHz Signal Bandwidth” IEEE Journal of Solid-State Circuits, **39** (2004) 75.

2. G. I. Bourdopoulos, A. Pnevmatikakis, V. Anastassopoulos, and T. L. Deliyannis, “Delta-Sigma modulators modeling, Design and Applications” Imperial College Press, London.

3. J. C. Candy, G. C. Temes, “Oversampling Methods for A/D and D/A conversion,” in Oversampling Delta-Sigma Data Converters, IEEE Press, (1992) 1.

4. P. M. Aziz, H. V. Sorensen, J. van der Spiegel, “An overview of sigma-delta converters,” **13** (1996) 61.

5. J. X. Przybysz , “Josephson Analog to Digital converters,” in ‘The new superconducting electronics’ edited by H. Weinstoch and R. Ralston, NATO ASI series, Kluwer Academic publications.

6. D. L. Miller, J. X. Przybysz, D. L. Meier, J. H. Kang and A. H. Worsham, “Characterization of a superconductive sigma-delta analog to digital converter,” IEEE Trans. Appl. Supercond., **5** (1995) 2453.

7. A. H. Sonnenberg, I. Oomen, H. Hilgenkamp, G. J. Gerritsma, and H. Rogalla, “Sigma-Delta A/D converter in HTS ramp edge technology,” IEEE Trans. Appl. Supercond., **11** (2002) 200.

8. J. X. Przybysz , D.L. Miller and E. H. Naviasky, “Two-Loop Modulator for Sigma-Delta Analog to Digital Converter,” IEEE Trans. Appl. Supercond., **5** (1995) 2248.

9. T. V. Flippov, Y. A. Polyakov, V. K. Semenov, and K. K. Likharev, “Signal resolution of RSFQ comparators,” IEEE Trans. Appl. Supercond., **5** (1995) 2240.

10. A.H. Sonnenberg , G.J. Gerritsma, H. Rogalla, “Balanced comparator fabricated in ramp edge technology,” Physica C, **326–327** (1999) 12.

11. B. Oelze, B. Ruck, M. Roth, R. Do¨mel, M. Siegel A. Yu. Kidiyarova-Shevchenko, T. V. Filippov, M. Yu. Kupriyanov G. Hildebrandt, H. Topfer, and F. H. Ihlmann, W. Prusseit, “Rapid single-flux-quantum balanced comparator based on high-Tc bicrystal Josephson junctions,” Appl. Phys. Lett., **68** (1996) 2732.

12. E. S. Fang and T. V. Duzer, “A Josephson integrated circuit simulator (JSIM) for superconductive electronics application,” ISEC89.

13. A. H. Worsham, D. L. Miller, P. D. Dresselhaus, A. H. Miklich, and J. X. Przybysz, “Superconducting modulators for high dynamic range Delta-Sigma analog-to-digital converters,” IEEE Trans. Appl. Supercond., **9** (1999) 3157.

14. B. E. Boser and B. A. Wooley, “Design of sigma-delta modulation analog-to-digital converters,” IEEE journals of solid state circuits, **32** (1998) 1298.

15. T. Hashimoto, H. Hasegawa, S. Nagasawa, H. Suzuki, K. Miyahara, Y. Enomoto, “Superconducting second-order delta-sigma modulators utilizing multi-flux-quantum generators,” IEEE Trans. Appl. Supercond., **11** (2001) 554.

Chapter 5

Pulse stretcher design and realization

5.1 Introduction

In RSFQ circuits, data are sent in the form of SFQ pulses. The small amplitude, the very short pulse width of few picoseconds and the high speed of several GHz prohibit a direct transfer of SFQ pulses to semiconducting circuits. Therefore one needs RSFQ circuits that at least provide an extended voltage pulse with a significant increase in the voltage level and reduced speed. The Impedance mismatch problem has to be considered as well. A number of possible solutions has been developed and tested in niobium technology. SFQ-to-latch converters [1], voltage multipliers [2], SQUID amplifiers [3] and SFQ-to-DC converters [4] are some of the interesting circuits, that could in principle be applied to the problem. Some of the circuits need more than one stage, some need un-shunted junctions and for some circuits the spread in the critical current of junctions is more important, so that a careful analysis has to be made when circuits are implemented in HTS technology. A SFQ-DC converter with a set and a reset pulse (pulse stretcher) can be used because of the small number of junctions offering a significant yield even with a large spread in the critical current. Pulse stretchers are commonly used to monitor SFQ pulses in RSFQ circuits. The pulse stretcher gives an extended voltage pulse with the time period set by the proper application of set and reset pulses. The output voltage is limited by the $I_C R_N$ product of the output junction (around 1mV). So, an ultra low noise, wideband, low input impedance semiconducting amplifier will be needed in order to process the data by room temperature electronics.

5.2 Circuit design and simulation

Two possible pulse stretcher designs have been considered in detail. The schematic of the first design is given in figure 5.1.

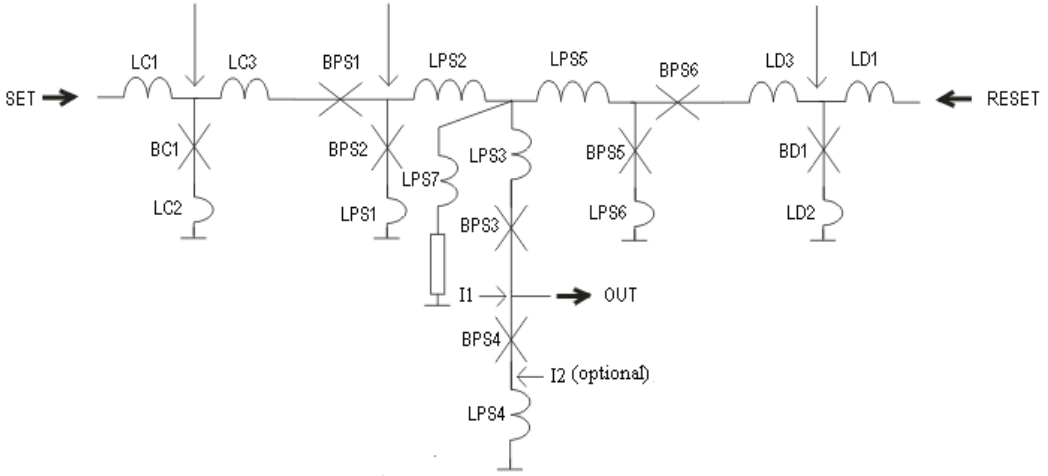


Figure 5.1: Pulse stretcher-design 1 [5].

The design consists of a quantizing loop interrupted by two junctions BPS2 and BPS5 with the inductors LPS2 and LPS5. At the node connecting LPS2 and LPS5, two junctions BPS3 and BPS4 are connected in series to ground. Initially, the value of the bias current will be chosen such that the junction BPS4 will be in the voltage state. The effect of every fluxon emitted across junction BPS4 will be balanced by the anti-fluxon generated across junction BPS3. The initial state of the loop will be stable until junction BPS2 switches by applying a set pulse. This causes a phase increase along junctions BPS3 and BPS4. The additional current due to the phase increase prevent the anti-fluxon generation. Junction BPS4 then returns to the zero-voltage state. This state will continue until a reset pulse is applied across BPS5. Reset pulse will causes an additional current along BPS4. Now BPS4 will start switching. The circulating current plus the diverted bias current is then enough for an anti-fluxon to be generated. BPS4 will be in the voltage state continuously until setting the loop. With an optional bias current I2, the initial state of junction BPS4 can be changed to the zero-voltage state. The JSIM simulation of this pulse stretcher is shown in figure 5.2.

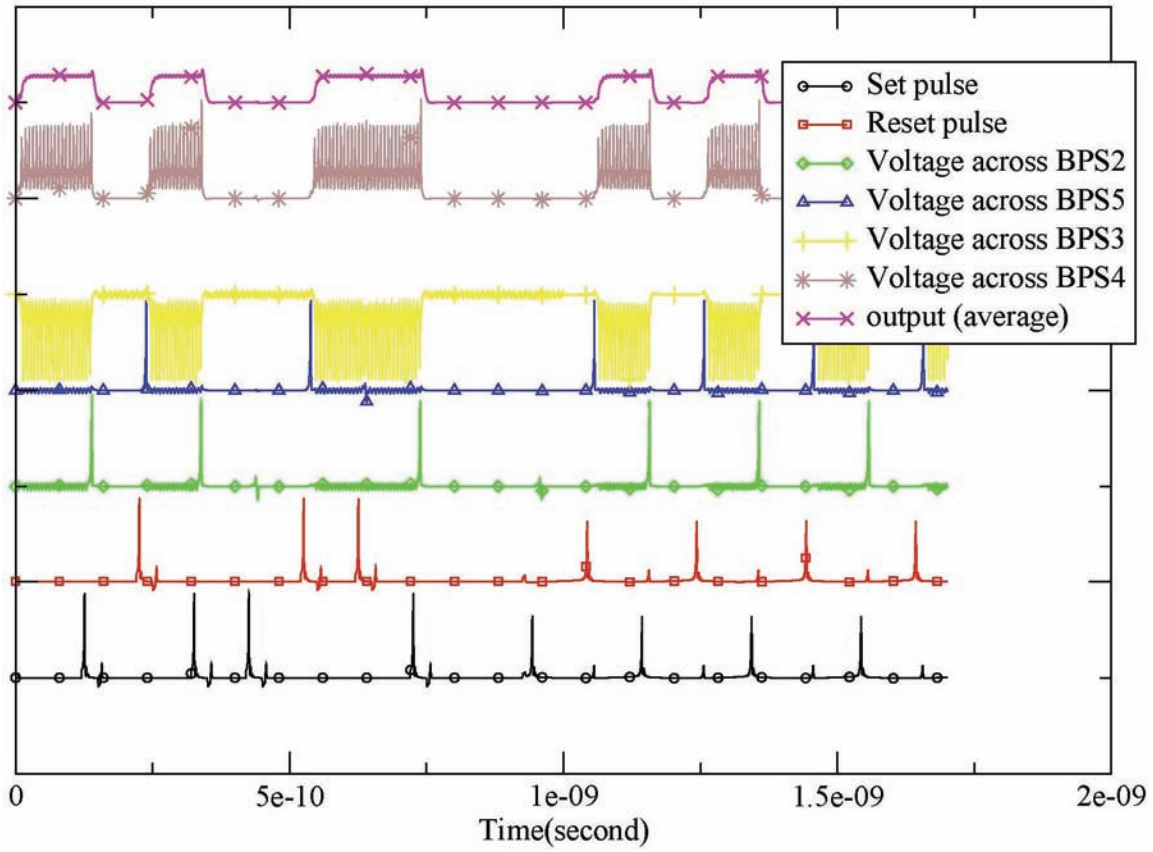


Figure 5.2: Simulation of pulse stretcher-design 1.

The correct operation of the circuit is verified by the simulation. A set of optimized values for the first design is given in table 5.1.

LC1 =2.4pH	BC1 =312μA
LC2 =1.2pH	BPS1 =216μA
LC3 =3.0pH	BPS2 =320μA
LPS1 =1.2pH	BPS3 =220μA
LPS2 =4.5pH	BPS4 =185μA
LPS3 =1.2pH	BPS5 =312μA
LPS4 =1.0pH	BPS6 =185μA
LPS5 =5.2pH	BD1 =312μA
LPS6 =1.2pH	
LPS7 =2.0pH	RPS1 =1 Ω
LD1 =3.0pH	
LD2 =1.2pH	
LD3 =3.0pH	

Table 5.1: Optimized parameters of pulse stretcher design 1.

The margin for each parameter is shown below in figure 5.3.

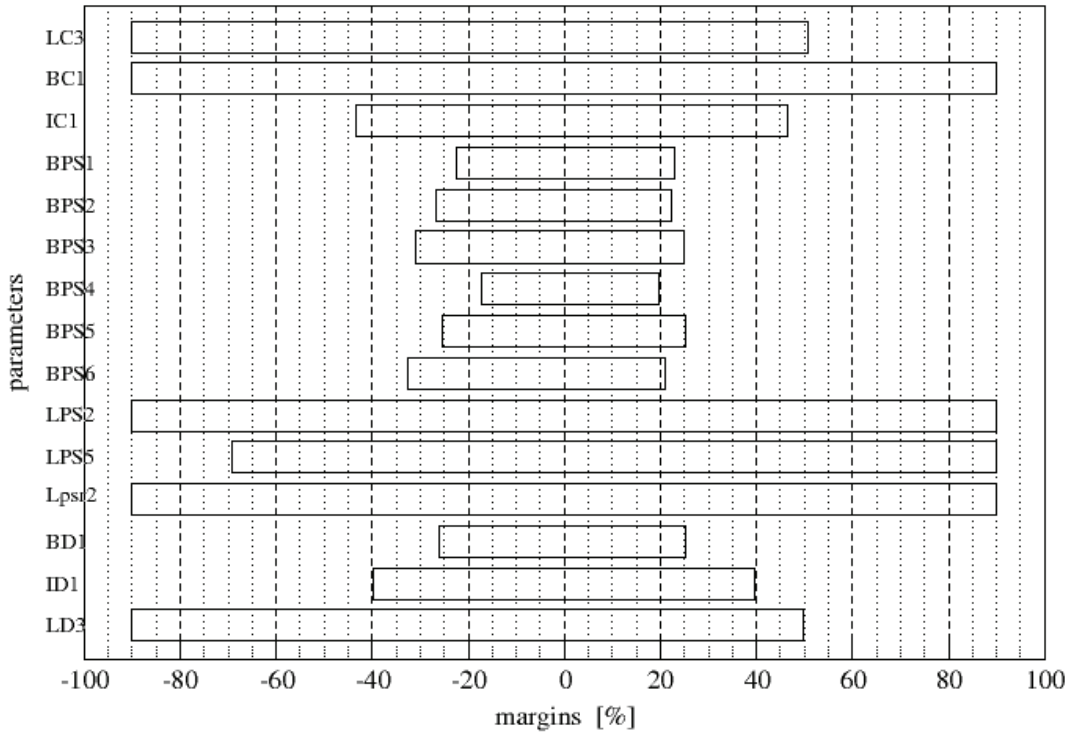


Figure 5.3: Pulse stretcher margin calculation.

In the next design (figure 5.4), an inductor LPS8 is coupled mutually with the inductor LPS2 of the SQUID comprising junctions BPS2 and BPS5. One end of LPS8 is connected to ground through the two junctions BPS3 and BPS4 in series. Another end is grounded through an inductor. Buffer junctions are included to avoid false pulses at the set and reset terminal that can affect the state of the storage loop.

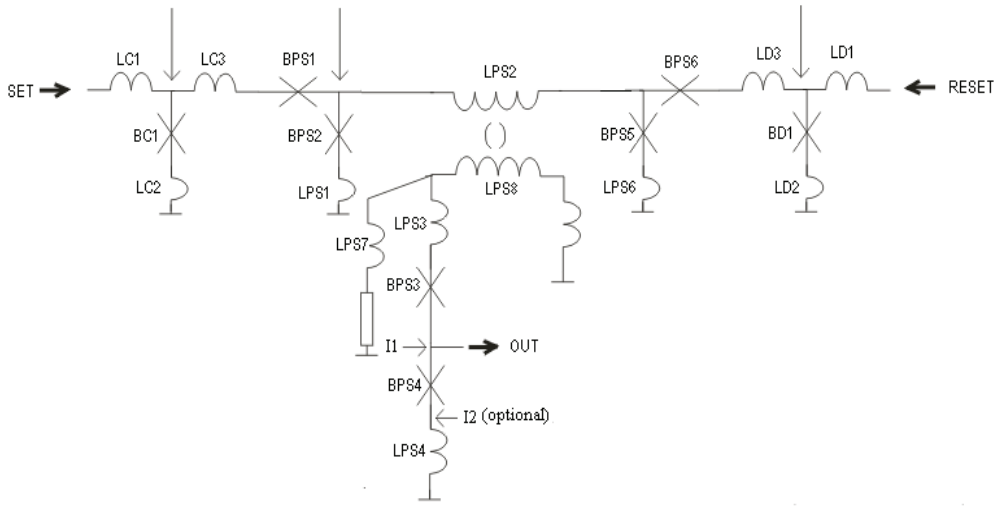


Figure 5.4: Second pulse stretcher design.

The parameters of both designs have been optimized to obtain maximum margins. For the second design, a coupling constant of value 0.6 was used between the inductor LPS2 and LPS8. During the yield analysis, bias currents are fixed by the values obtained from the margin calculation. Figure 5.5 shows the relation between the one sigma spread and the fabrication yield for both the designs. Based on this analysis, design 1 which has a higher yield, was used for further studies.

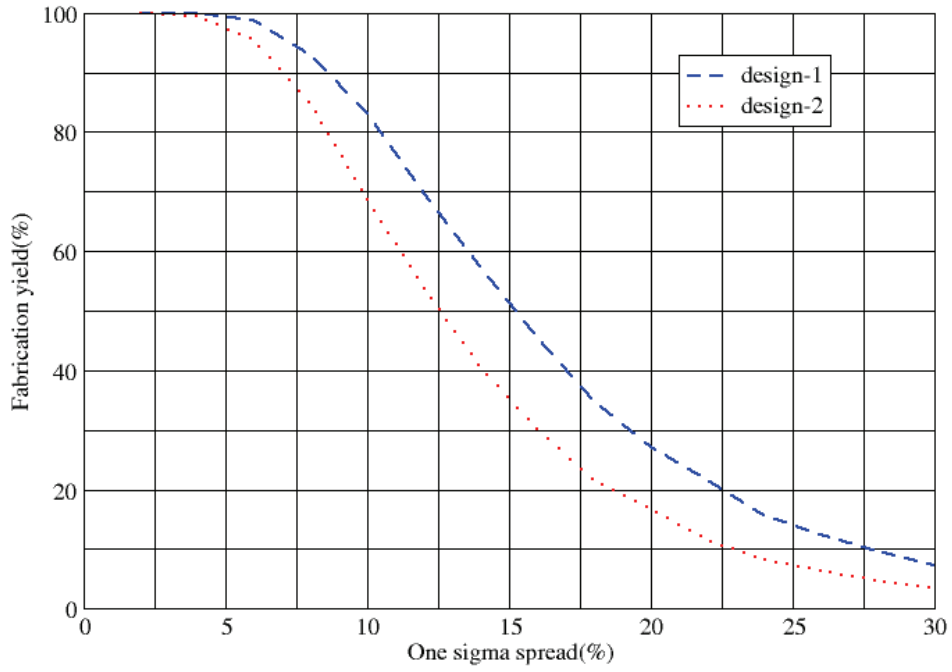


Figure 5.5: Fabrication yield of both pulse stretchers.

5.3 Pulse stretcher fabrication

From the results obtained from the junctions and SQUID experiments, a pulse-stretcher circuit was designed and simulated. We have optimized the circuit design and designed a mask to utilize non-rotating etching. Since there is no provision for cooling substrate holder during rotating etching, the excess heat produced during etching affects the superconducting property of the electrode. In the new design, all junctions are placed on ramps facing the same direction. Another mask layout has been designed for utilizing rotating etching and it is given in appendix 2. The schematic of the circuit is shown in figure 5.6.

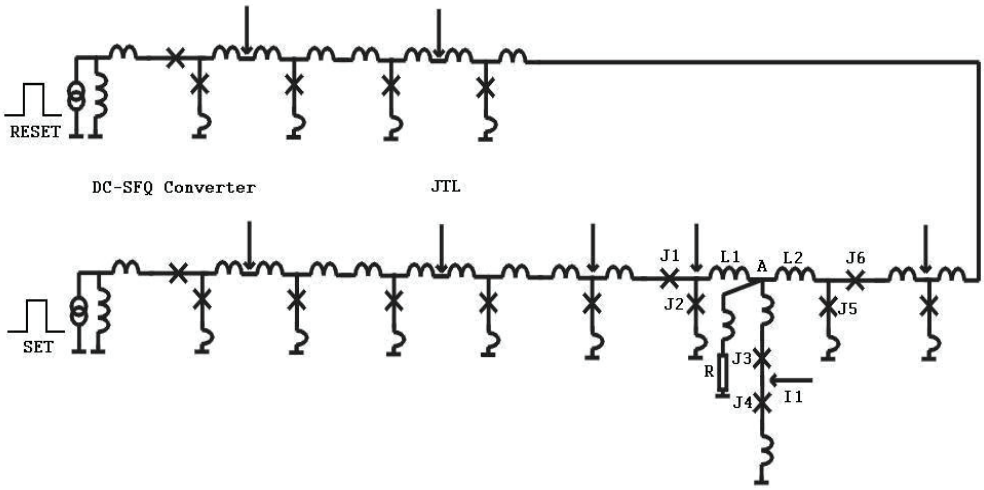


Figure 5.6: Schematic of the fabricated pulse stretcher circuit.

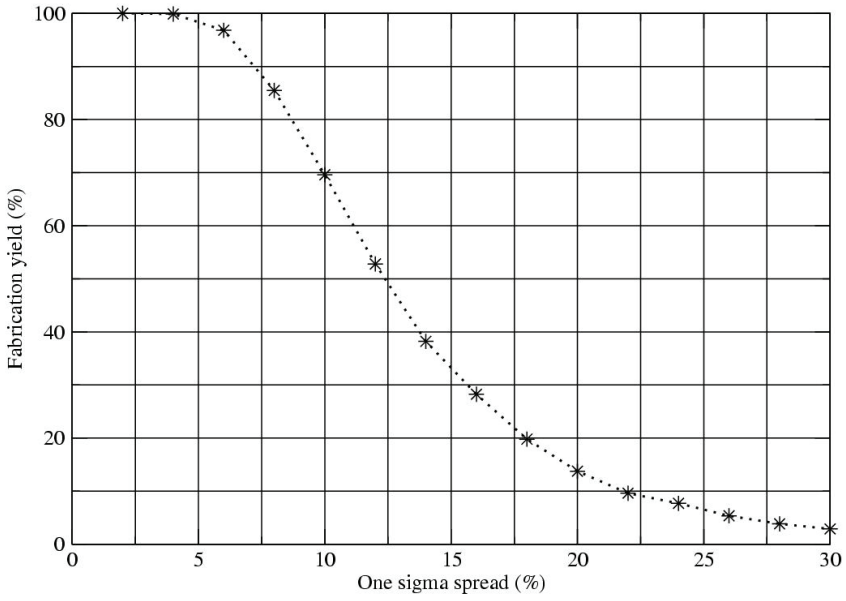


Figure 5.7: Fabrication yield of the pulse stretcher as a function of one sigma spread.

The circuit was optimized using the tool XOPT in order to reach a maximum fabrication yield. Set and reset pulses are generated by DC/SFQ converters and applied to the pulse stretcher via JTLs. The junctions J1 and J6 are the buffer junctions to protect junctions J2 and J5 from false pulses from the input sides. The output is taken across junction J4. A plot between the one sigma spread and the yield is shown in figure 5.7.

The mask layout, as drawn by the Clewin program, is shown in figure 5.8. The output signal is measured via a coplanar line [6].

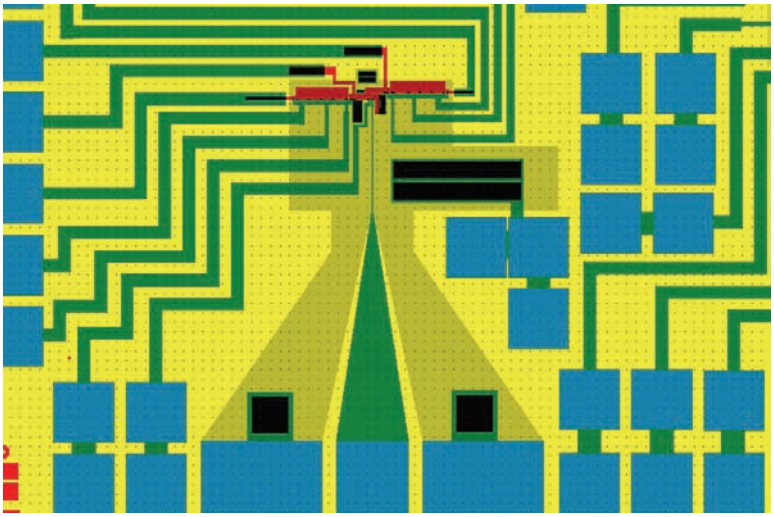


Figure 5.8: Mask layout.

The steps involved in the fabrication of the pulse stretcher are described in chapter 2. An optical photograph of the fabricated sample is shown in figure 5.9.

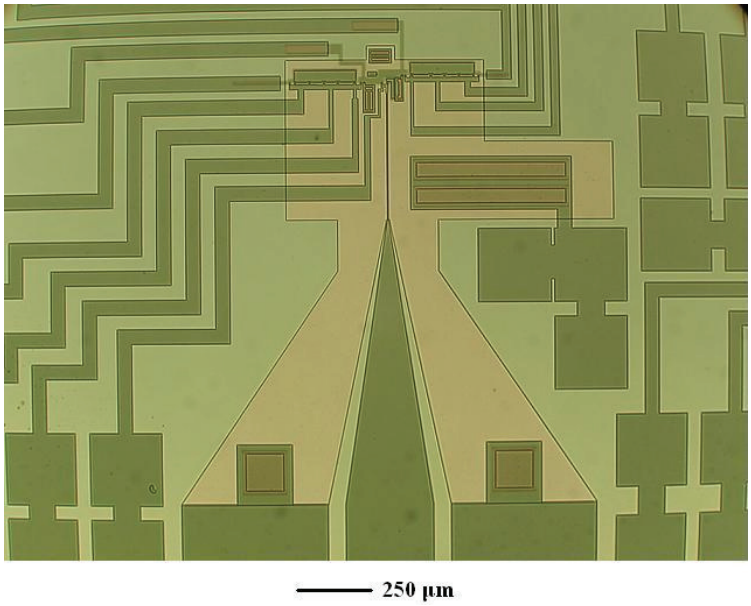


Figure 5.9: Optical photograph of the pulse stretcher sample.

5.4 Measurement results

For characterization, a fabricated sample is glued on a chip carrier and mounted on a sample rod (probe) and inserted into a continuous flow cryostat which can cool down to a temperature of 2 K. the temperature inside the cryostat can be controlled by regulating the Helium flow by a rotary pump and a PID controlled heater. The sample rod contains 22 filtered current lines through which bias currents to the sample are applied by a computer controlled current source. There are 22 voltage lines that one amplified by a low noise amplifier. The part of the sample rod where the sample is placed, is shielded by a μ metal cylinder.

The fabricated circuit consists of 13 junctions and 10 bias lines. From the inductance measurement and junction I-V characteristics at different temperatures, one can find out the correct operating temperature, at which the LI_C products for storage loop and non-storage loops are close to the designed values. The optimal operating temperature was found to be 47 K. A measurement of the pulse stretcher at 47 K is shown in figure 5.10.

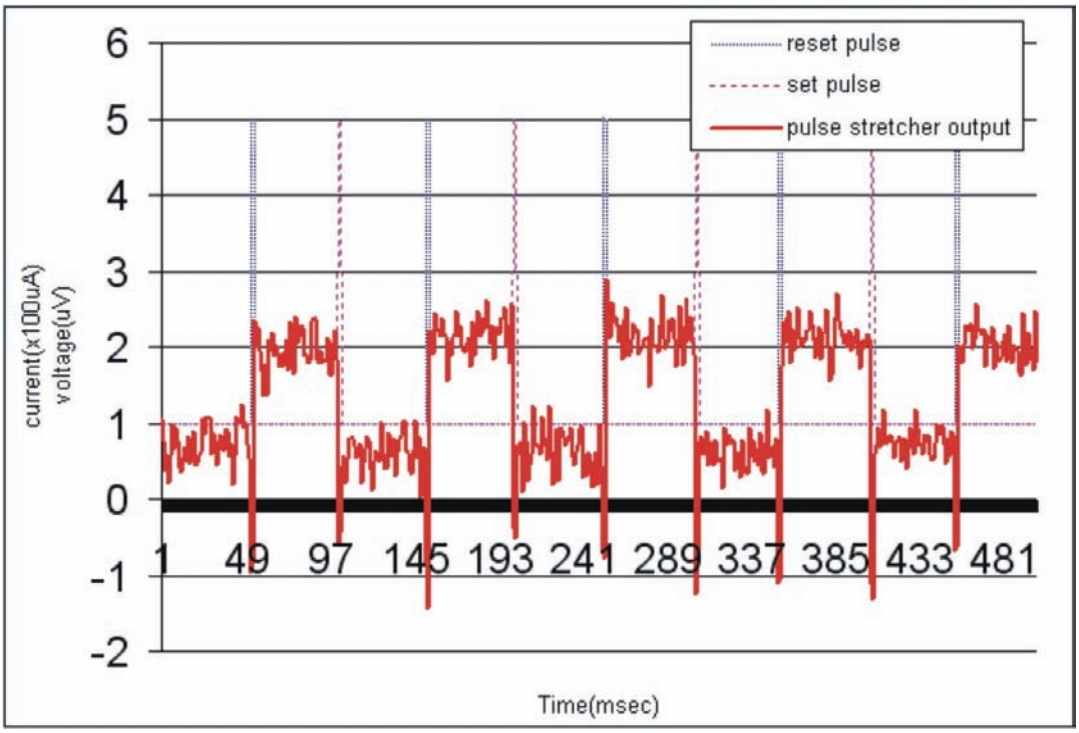


Figure 5.10: Measurement of a pulse stretcher.

A low output voltage is connected to the current level at the node connecting J3 and J4 and dependence of the $I_C R_N$ product on temperature. The correct operation of the pulse stretcher was strongly affected by the bias current *I1* (figure 5.6). A 5% change in *I1* introduced malfunctioning of the circuit. In some of the fabricated chips, the state of the storage loop was changing randomly without depending on the set and reset pulses.

This might be due to thermal switching and noise in the measurement setup along with the spread in the junction parameters which reduce the chance of correct operation. A maximum output voltage of 90 μV was obtained for a sample measured around 19K, but with switching errors.

Placing junctions in the same ramp direction causes an increase in the parasitic inductance between the junctions in pairs (J1, J2), (J3, J4) and (J5, J6). Hence, the fabrication yield has been reduced further for a 10% spread in the technology.

5.5 Conclusion

Simulations of pulse stretcher designs, calculations of their parameter margins and optimization with respect to the spread in the fabrication process were studied. The pulse stretcher can be integrated easily with other RSFQ circuit elements such as a comparator, modulator without affecting their circuit function. In the case of interfacing with the semiconducting electronics, the maximum output data rate of the RSFQ circuit is limited by the bandwidth of the semiconducting amplifier. As the pulse stretcher output is determined by the $I_C R_N$ product of the output junction, the amplifier should also have a high sensitivity in detecting low signals.

The correct operation of the pulse stretcher has been tested experimentally in HTS technology. The design rules and the fabrication techniques introduce parasitic elements and additional parameter spread reducing the fabrication yield of the circuit.

References

1. J. X. Przybysz, D. L. Miller, S. S. Martinet, J. Kang, A. H. Worsham, and M. L. Farich, “Interface circuits for chip-to-chip data transfer at GHz rates,” IEEE Trans. Appl. Supercond., **7** (1997) 2657.

2. V. Semenov, “Digital-to-Analog conversion based processing of SFQ pulses,” IEEE Trans. Appl. Supercond., **3** (1993) 2637.

3. O. A. Mukhanov, S.V. Rylov, D. V. Gaidarenko, N.B. Dubash, and V.V. Borzenets, “Josephson output interfaces for RSFQ circuits,” IEEE Trans. Appl. Supercond., **7** (1997) 2826.

4. V. K. Kaplunenko, M. I. Khabipov, V. P. Koshelets, K. K. Likharev, O. A. Mukhanov, V. K. Semenov, I. L.Serpuchenko and A. N. Vystavkin, “Experimental study of the RSFQ logic elements,” IEEE Trans. On Magnetics, **25** (1988) 861.

5. K. K. Likharev, and V. K. Semenov, “RSFQ logic/memory family: A new Josephson-junction digital technology for sub-terahertz-clock-frequency digital systems,” IEEE Trans. on Appl. Supercond., **1** (1991) 3.

6. S. S. Bedair and I. Wolf, “Fast, accurate and simple approximate analytic formulas for calculating the parameters supported coplanar waveguides for (M)MICs,” IEEE Trans. Microwave Theory Tech., **40** (1992) 41.

Chapter 6

Interfacing the pulse stretcher to RSFQ and read-out circuits

6.1 Introduction

We have studied two models that can be used to connect the pulse stretcher to other RSFQ circuits. The connection has to be made in order to transfer SFQ data between superconductor and semiconductor electronics circuits. In a hybrid system, both Josephson and CMOS circuits are working at different voltage levels. Impedance matching is therefore necessary to transfer maximum power with minimum reflections at the interface. The JSIM simulator was used to study the interfacing effect.

6.2 RSFQ – pulse stretcher interface

6.2.1 Internal set and reset model

This model includes one DC/SFQ converter, one splitter, Josephson transmission lines and one comparator, as shown in figure 6.1.

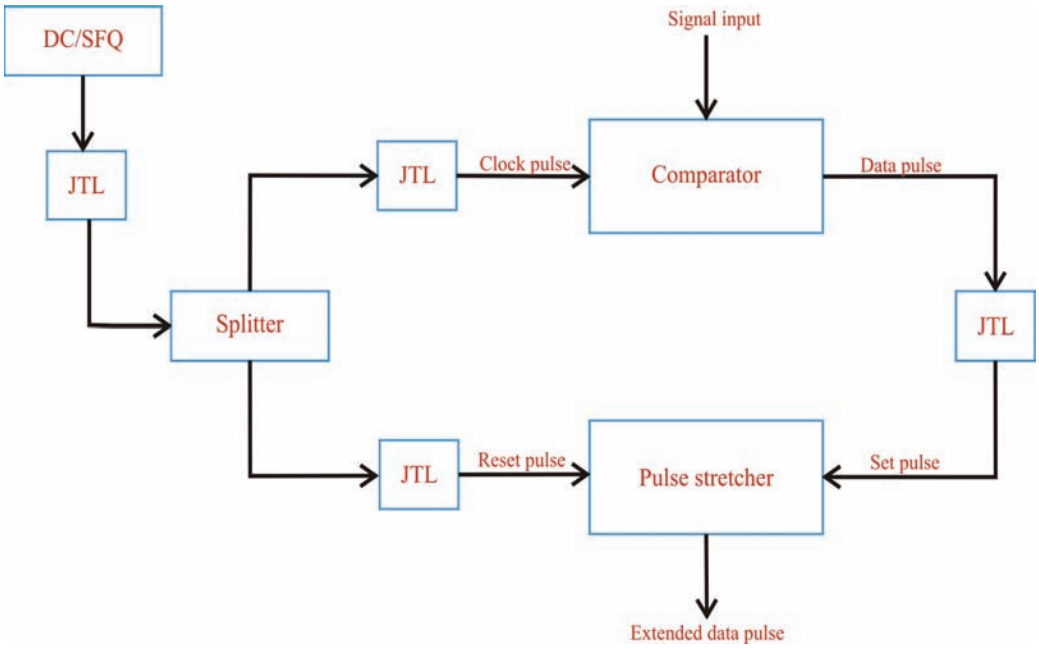


Figure 6.1: Pulse-stretcher based on internal set and reset pulses.

The model operates as follows. From the DC/SFQ converter, SFQ pulses propagate through a JTL with the aim to improve the signal quality for driving a splitter. The splitter output signals are directed into two directions. One of the signals will reach the pulse stretcher reset input through a JTL. In parallel, the other signal will go through a comparator. If the comparator input current is higher or lower than a certain threshold

value, either the lower or upper junction of the comparator will switch in response to the sampling pulse. The output signal of the lower junction will be provided through a longer JTL to the pulse stretcher set input. Figure 6.2 shows the operation of this model of which simulation showed correct functioning.

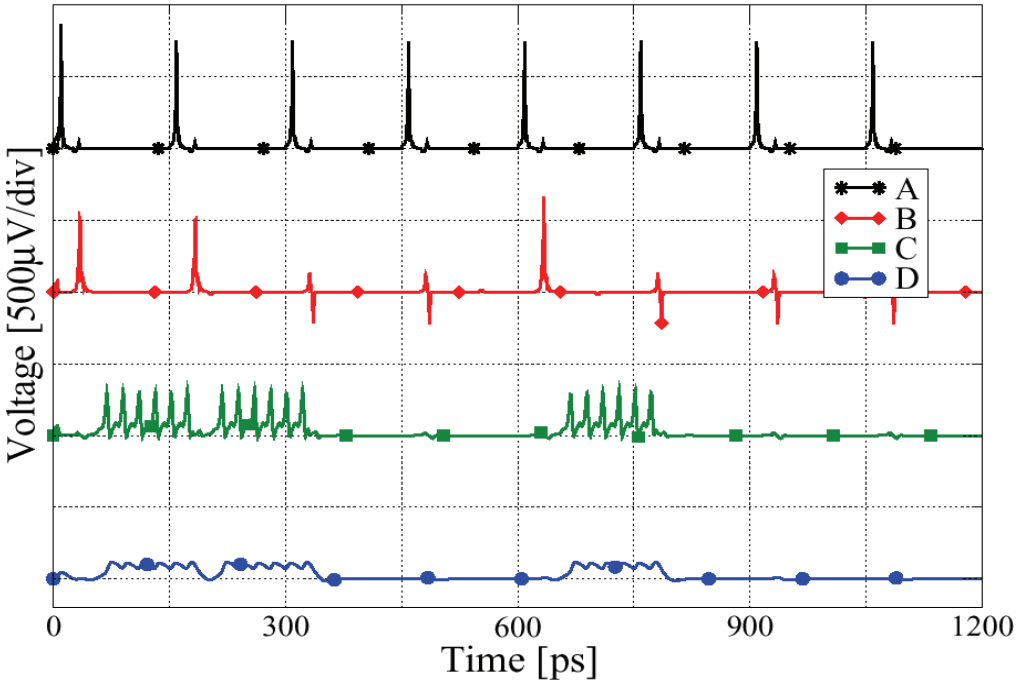


Figure 6.2: Simulation of the pulse stretcher with internal set and reset pulses (clock frequency=6GHz). The output signal corresponds to a bit stream of 11001000. Curve (A) represents the DC/SFQ output, (B) the comparator output, (C) voltage at the pulse-stretcher output junction and (D) the pulse stretcher average voltage output.

Optimization of this circuit yields critical margins of ± 10–15%. This model is very interesting because everything is fixed by the design itself: the delay between set and reset signals as well as the timing characteristics of the comparator. All these parameters are fixed by the clock input frequency. This circuit includes 28 junctions but only a few of them are critical. The reset pulse should arrive at the pulse stretcher before the set pulse. We calculate a timing jitter of $\sigma = \pm 0.46\,\text{ps}$ per junction. By counting 6 junctions in the path JTL+splitter+JTL, this yields a timing window of $5\sigma = \pm 5.63\,\text{ps}$. This timing demands a set pulse to arrive approximately 6 ps after the reset pulse. Since the output voltage of the pulse-stretcher is too low (only 150 μV) for being detected by a semiconducting amplifier, a superconducting amplifier stage can be added to further increase the output voltage.

6.2.2 External reset model

As an alternative design, a second clock signal could be used as a reset signal. The delay can be placed outside the HTS chip, thereby decreasing the number of junctions. This model includes two DC/SFQ converters, Josephson transmission lines, a comparator and the pulse-stretcher (figure 6.3). Each DC/SFQ converter is fed by a sinusoidal input signal, but with a phase difference of 180 degrees.

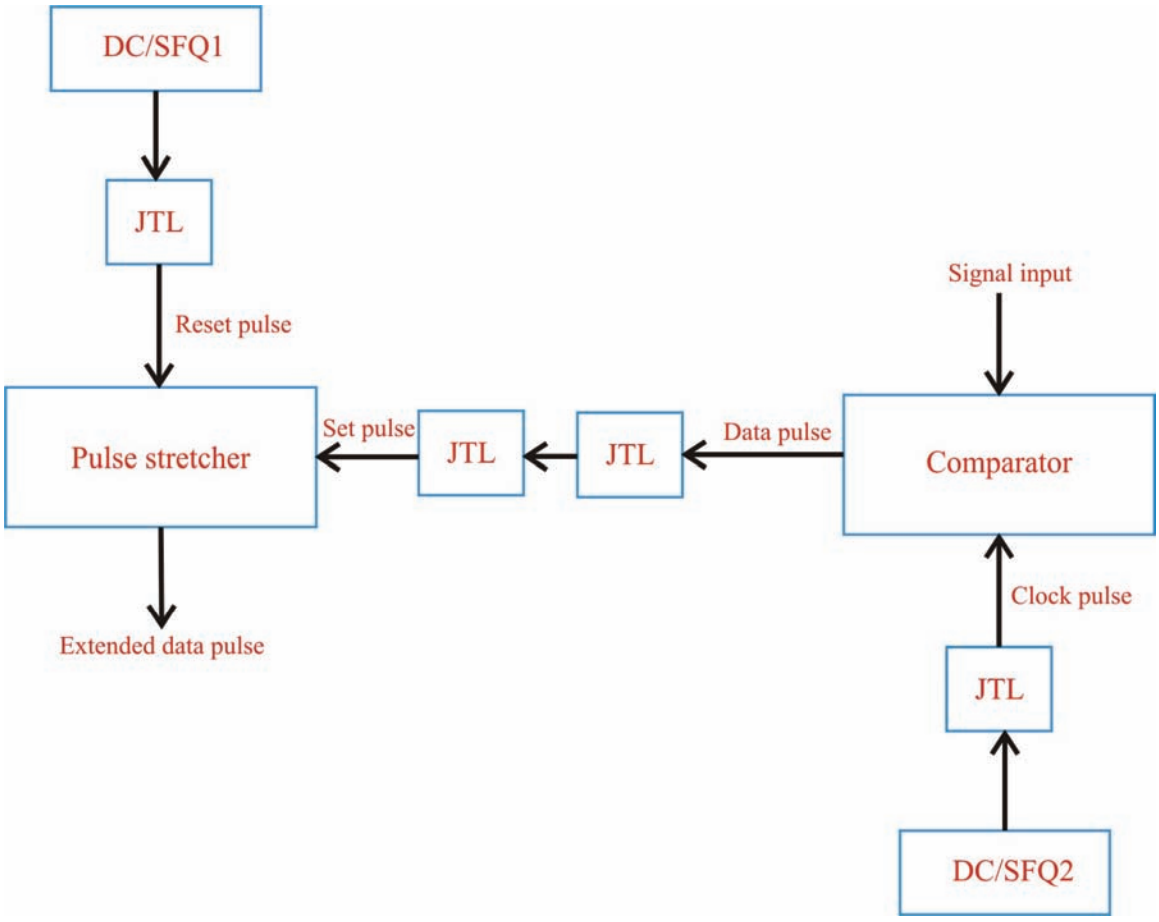


Figure 6.3: Pulse stretcher interface with an external reset pulse.

The output signal from the DC/SFQ1 output, through a JTL reaches the reset port of the pulse-stretcher input. Half a period later, the signal from the DC/SFQ2 output reaches the comparator stage. As previously explained, depending on the comparator output, its output signal will set the pulse-stretcher output. Figure 6.4 shows the simulation of this model.

The optimization of this circuit yields lower margin requirements than the first model, with ± 15%. The circuit includes 24 junctions. To conclude, the operation of the second model is simpler than that of the first model at the cost of a not totally internal set and reset circuit. In terms of energy losses and performance, a better behavior is expected from the first model. Although its fabrication will be more critical than the fabrication of the second model, in the case of a practical implementation in the global circuit, the first model is the better choice.

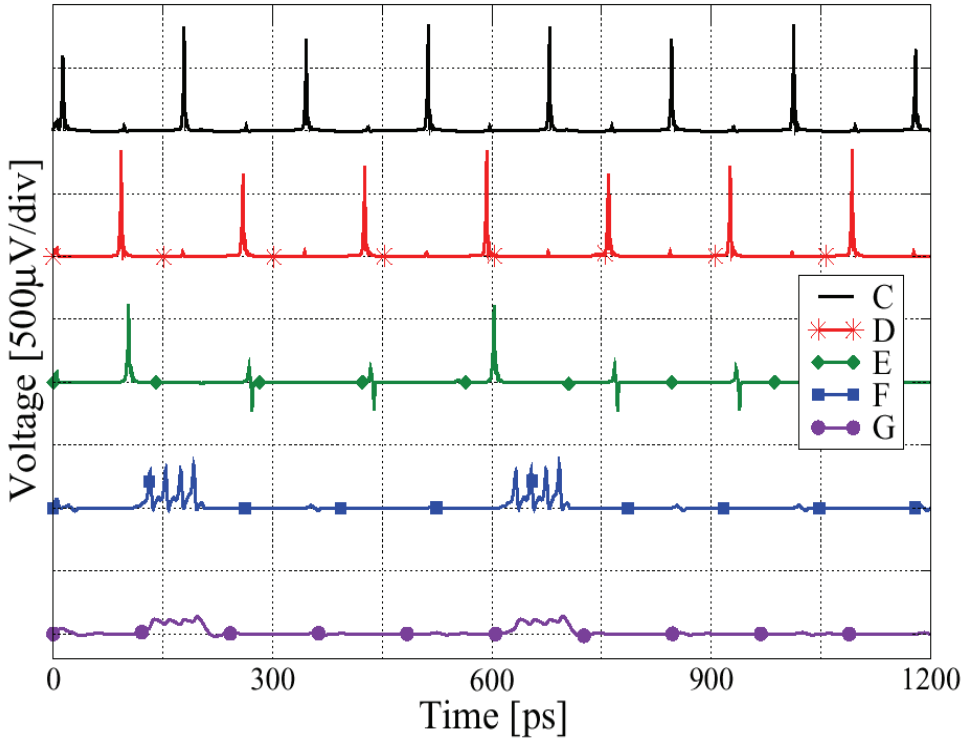


Figure 6.4: Simulations of the second set reset Pulse stretcher model (6GHz). The output signal corresponds to a bit stream of 1001000. Curve (C) represents the DC/SFQ1 output, (D) the DC/SFQ2 output, (E) the comparator output, (F) the voltage at the pulse-stretcher output junction and (G) the pulse-stretcher average voltage output.

6.2.3 Simulation of the complete modulator - pulse stretcher circuit

The aim of studying the pulse stretcher was to use it as an interfacing circuit between the delta-sigma modulator and semiconducting circuits, to process the data from the modulator. The pulse stretcher has been simulated in combination with the 1st order delta-sigma modulator to get an extended pulse for every modulator output. Figure 6.5 shows the block diagram of the design.

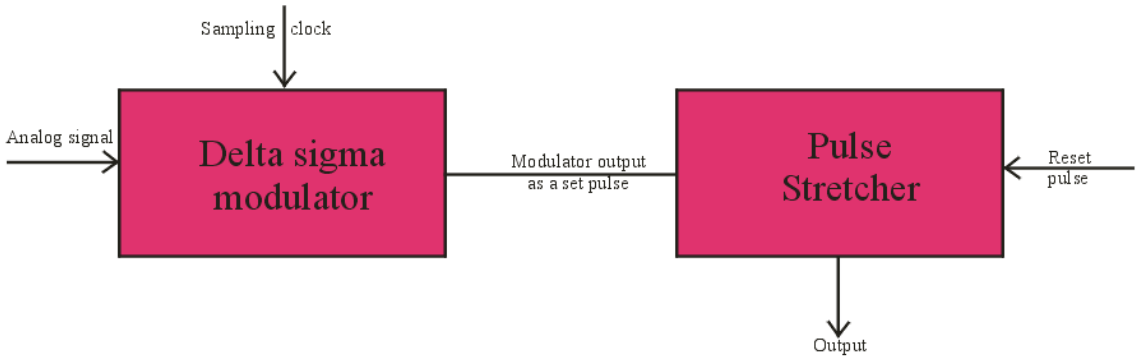


Figure 6.5: A block diagram of a delta-sigma modulator connected to a pulse stretcher.

Initially, the pulse stretcher output was fixed at zero voltage by the application of the optional bias current, as described in the pulse stretcher design section (5.2). A sampled data pulse of the delta-sigma modulator sets the pulse stretcher. Now, the pulse stretcher is in the voltage state. A reset pulse is applied before the next sampling pulse. Hence, the length of the voltage pulse of the pulse stretcher is mainly limited by the sampling time. The JSIM simulation results are shown in figure 6.6.

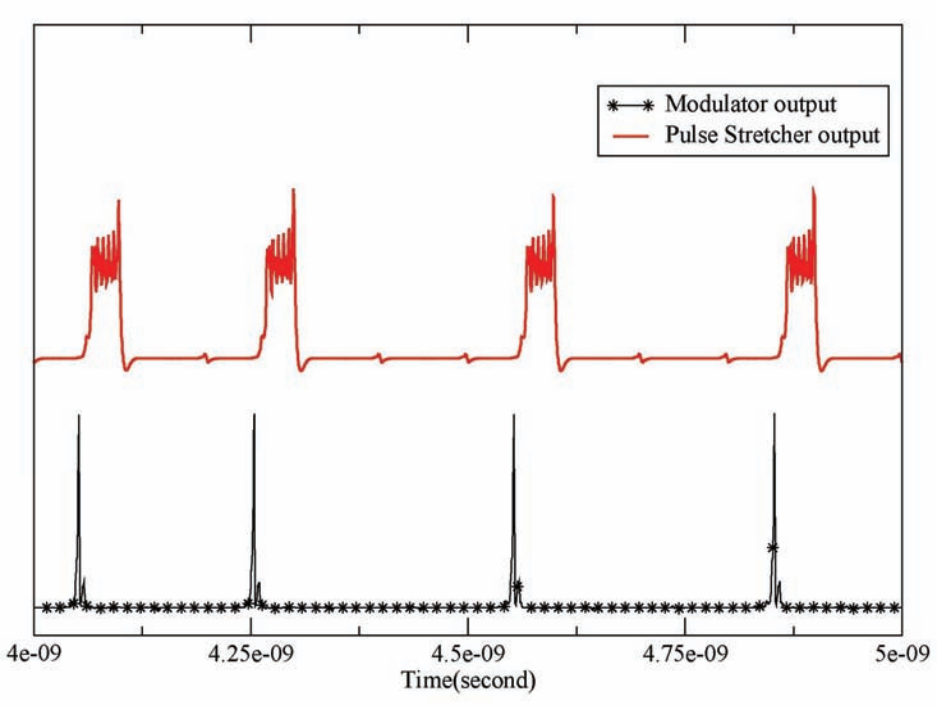


Figure 6.6: Simulation of a modulator connected to a pulse stretcher.

For the design, basic cells (DC/SFQ converter, JTL and comparator), which are described in appendix 1, are used. The margins of the pulse stretcher were not affected by the addition of the modulator. A designed mask layout is shown in appendix 2.

6.3 Pulse stretcher – read out interface

Inter-chip transmission of data is necessary to send SFQ data from the RSFQ circuit to the room-temperature electronics. At first, SFQ pulses are transformed into extended voltage pulses by the pulse stretcher. In general, circuits are placed away from the edges of the substrate to avoid any inhomogeneities during the junction process steps. As we use 10×5 mm^2 substrates, a passive line of minimum length of about 2 mm is enough to transport pulses to the edge of the chip. The propagation delay time of a passive line is an order of magnitude smaller than that of a JTL of the same length biased with 74% of critical current [1]. A very short length of wire bonding or flip-chip interconnection can be applied to transfer the data to another chip. As the voltage level at the output of the pulse stretcher is in the range of 100 μV-1 mV, care must be taken to minimize the impedance mismatch to reduce reflections back into the pulse stretcher. To reduce the parasitic inductance for a high data rate, the length of the wire and the height of the solder bump connector should be as small as possible [2].

Simulations have been performed to study the characteristics of the extended voltage pulse transmitted from the pulse stretcher to the passive transmission line terminated by a resistive load. We also studied the stability of the function of the pulse stretcher due to the reflections caused by the impedance mismatch. The block diagram of a test circuit is shown in figure 6.7.

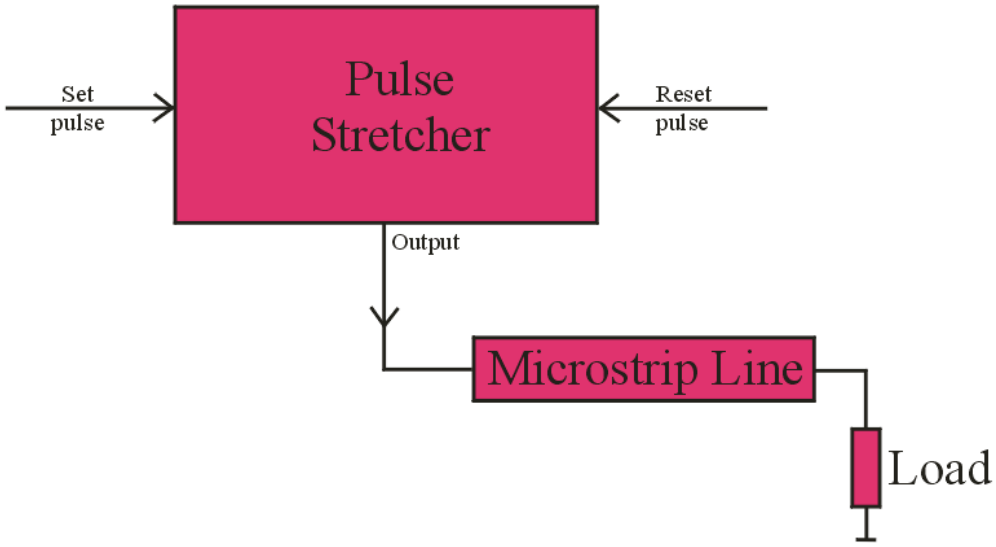


Figure 6.7: Block diagram of a pulse stretcher connected to a load resistor.

The critical current of the pulse stretcher output junction was 195 μA with an $I_C R_N$ product of 600 μV. For the calculation of the characteristic impedance, the dielectric constants of STO and PBCO were taken as 300 and 20 respectively. The impedance of 4 and 5 μm wide micro-strip lines are estimated to be 7.8 and 6.2 Ω respectively. Transmission of voltage pulses up to 20 GHz has been tested. The simulation results of the extended voltage pulses traveling via a 4 μm wide strip line of length about 2 mm

connected to a resistive load are shown in figure 6.8. To smoothen the output wave form, an LC filter was used in the simulation.

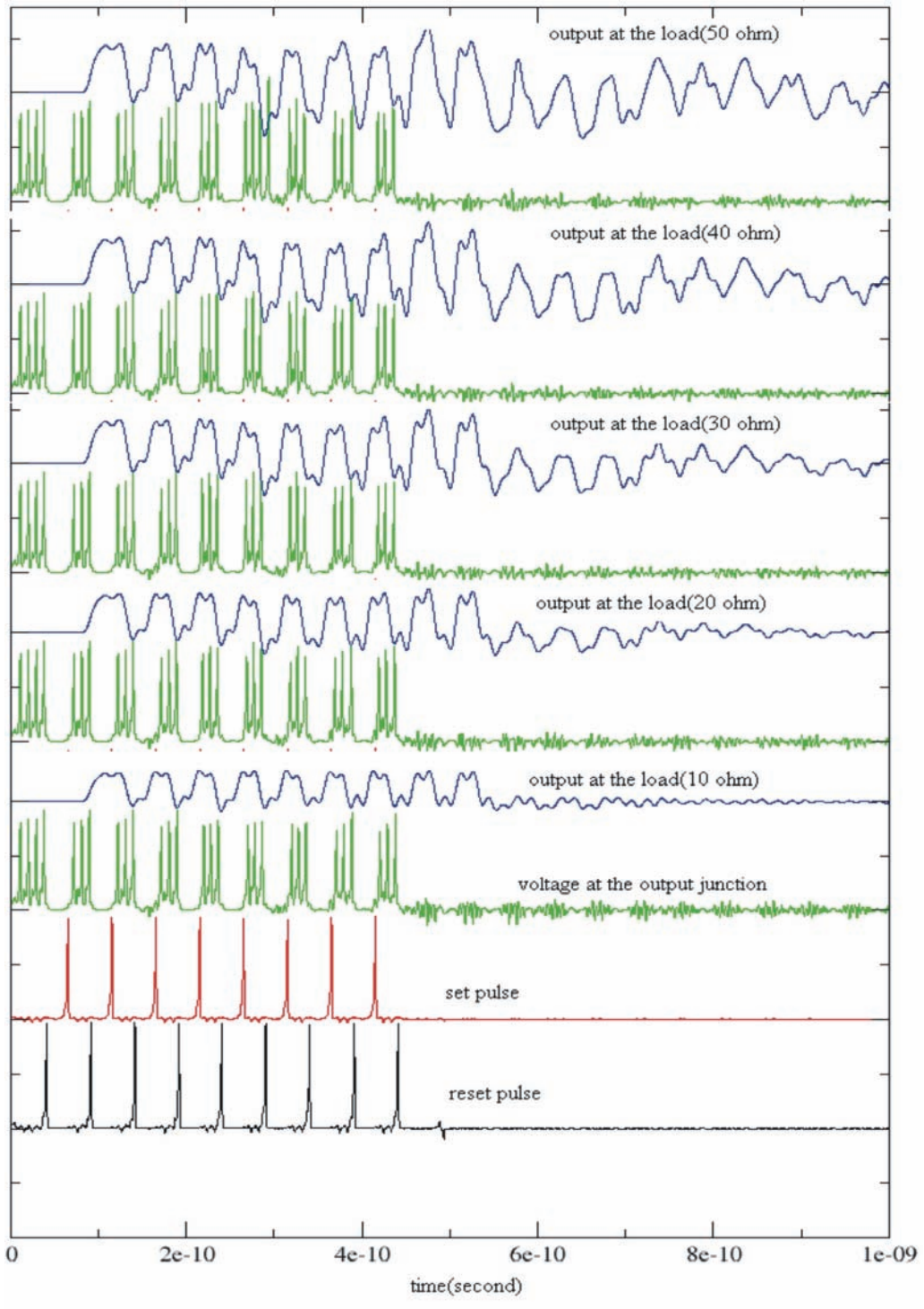


Figure 6.8: Simulation waveforms of the pulse stretcher connected to a 2 mm length micro-strip line terminated with different loads at a frequency of 20 GHz.

It was found that an increase in impedance mismatch causes an increase in the voltage of the reflected pulses. The pulse stretcher was stable for a load range of 10 - 50 Ω applying a 4 μm wide micro-strip line. The width of the strip line should be small to match with the high impedance load.

A HEMT amplifier can be operated above 100 GHz with very low noise performance below the liquid nitrogen temperature [3]. HEMT stands for High Electron Mobility Transistor. In a HEMT, a lattice matched hetero-junction is formed between two materials with different band-gaps. In a GaAs/AlGaAs hetero junction, the donor layer of n-AlGaAs (wide band-gap) supplies electrons for the conduction. These electrons are available in the lowest energy state at the GaAs (narrow band-gap) side. Since the thickness of the GaAs layer is much smaller than the de Broglie wavelength of the electrons, a two dimensional high mobility electron gas is formed in the narrow band gap material at the junction. A bias applied to the gate controls the conductivity of the device. These amplifiers can be matched with RSFQ circuits with an input stage that is terminated with a low input impedance (close to that of a HTS Josephson junction) at the cost of gain reduction [4].

6.4 Conclusion

Two models for using a pulse stretcher as an interfacing element between an RSFQ circuit and semiconducting circuits have been described. In the first model, delays between the set and reset terminals are determined by the Josephson transmission lines that consume more junctions than for the second model. Since in the second model, the reset pulse is applied externally, the design is more flexible with larger margin than the first model. However, having a consistent internal reset has the preference in most applications.

A Josephson junction is easily matched with a superconducting passive transmission line. To study the interfacing with room temperature electronics, a simulation study has been done by sending extended voltage pulse along a micro strip line, terminated with a load resistor of values raging from 10 to 50 Ω. The amplitude of the reflected pulses is high for load resistances above 20 Ω. Therefore, a low input impedance semiconducting amplifier is required.

References

1. D. Gupta, Y.Zhang, “On-chip clock technology for ultrafast digital superconducting electronics,” Appl. Phys. Lett., **76** (2000) 3819.

2. T. Krems, W. Haydl, H. Massler, and J. Rudiger, “Millimeter-wave performance of chip interconnections using wire bonding and flip chip,” in IEEE Int. Microwave Symp., San Francisco, CA, **1** (1996) 247.

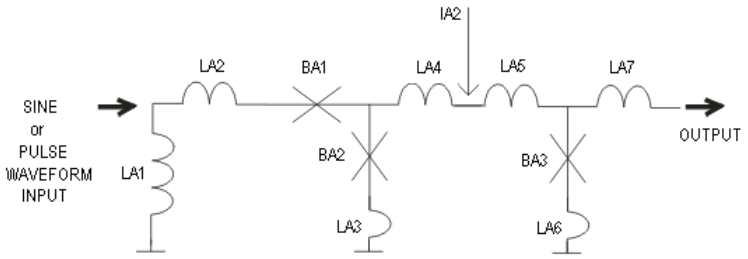
3. N. Wadefalk, A. Mellberg, I. Angelov, M. E. Barsky, S. Bui, E. Choumas, R. W. Grundbacher, E. L. Kollberg, R. Lai, N. Rorsman, P. Starski, J. Stenarson, D. C. Streit and H. Zirath, “Cryogenic Wide-Band Ultra-Low-Noise IF Amplifiers Operating at Ultra-Low DC Power,” IEEE Transactions on microwave theory and techniques, **51** (2003) 1705.

4. Super ADC annual report 2002.

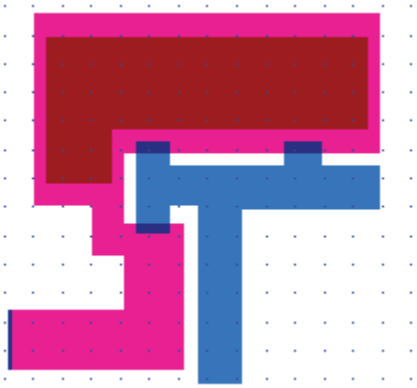
Appendix 1

RSFQ basic cells (design and mask layout)

Cell 1-DC/SFQ Converter



Circuit schematic-DC/SFQ converter

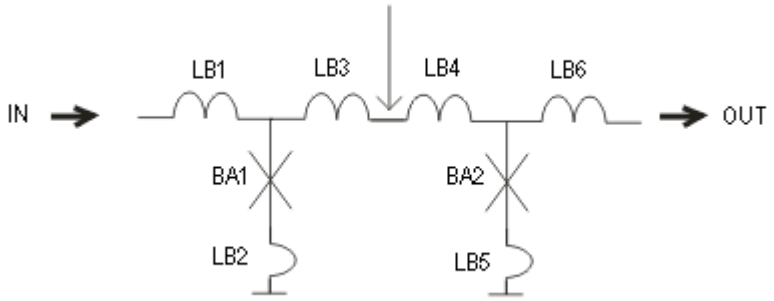


Layout- DC/SFQ converter

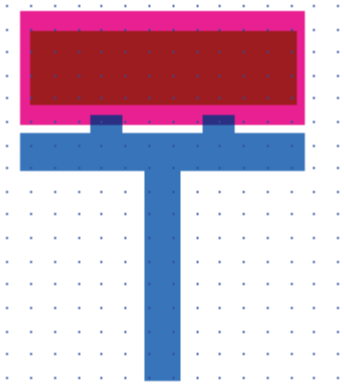
JSIM	Lmeter
LA1=2.8 pH LA2=1.8 pH LA3=1.5 pH LA4=1.5 pH LA5=2.0 pH LA6=1.2 pH LA7=2.0 pH BA1=215μA BA2=200μA BA3=240μA	LA1=2.777 pH LA2=1.762 pH LA3=1.640 pH LA4=1.565 pH LA5=2.170 pH LA6=1.173 pH LA7=2.025 pH

Table 1: parameters obtained from JSIM and Lmeter

Cell 2 - JTL



Circuit schematic-JTL

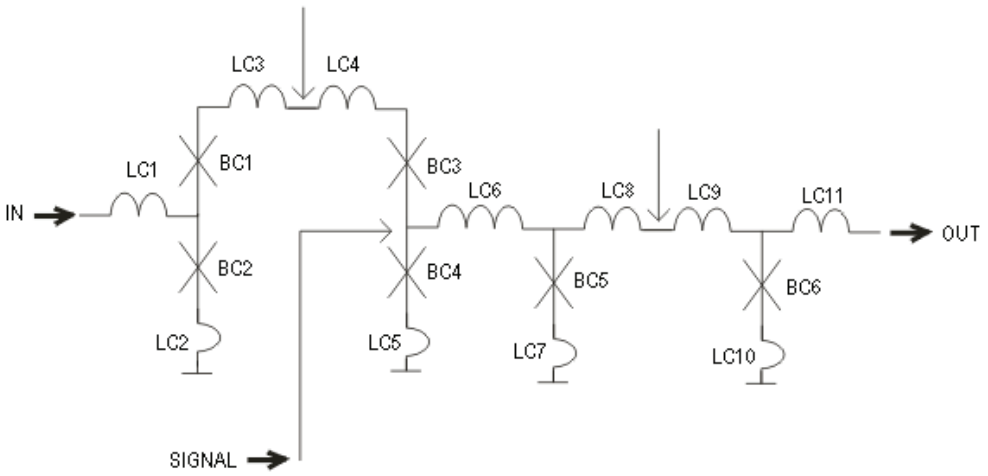


Mask layout-JTL

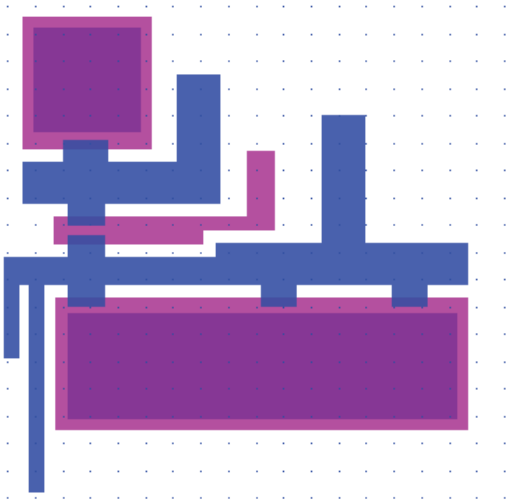
JSIM	Lmeter
LB1=1.8pH LB2=1.2pH LB3=1.8pH LB4=1.8pH LB5=1.2pH LB6=1.8pH BB1=250µA BB2=250µA	LB1=1.830 pH LB2=1.138 pH LB3=1.795 pH LB4=1.795 pH LB5=1.137 pH LB6=1.831 pH

Table 2: parameters obtained from JSIM and Lmeter

Cell 3-Comparator



Circuit schematic-Comparator



Mask layout- Comparator

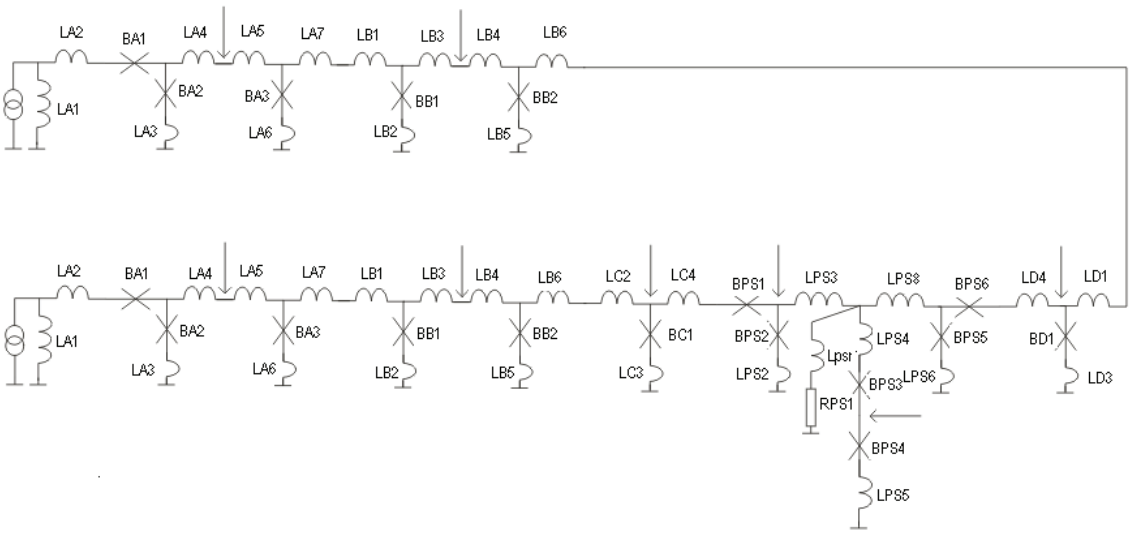
JSIM	Lmeter
LC1=1.8 pH	LC1=1.730 pH
LC2=1.2 pH	LC2=1.111 pH
LC3=2.0 pH	LC3=3.483 pH
LC4=2.0 pH	LC4=3.396 pH
LC5=1.2 pH	LC5=1.558 pH
LC6=7.0 pH	LC6=7.005 pH
LC7=1.2 pH	LC7=1.230 pH
LC8=2.0 pH	LC8=1.866 pH
LC9=2.0 pH	LC9=2.053 pH
LC10=1.2 pH	LC10=1.093 pH
LC11=1.8 pH	LC11=1.905 pH
BC1=320μA	
BC2=250μA	
BC3=270μA	
BC4=250μA	
BC5=250μA	
BC6=250μA	

Table 3: parameters obtained from JSIM and Lmeter

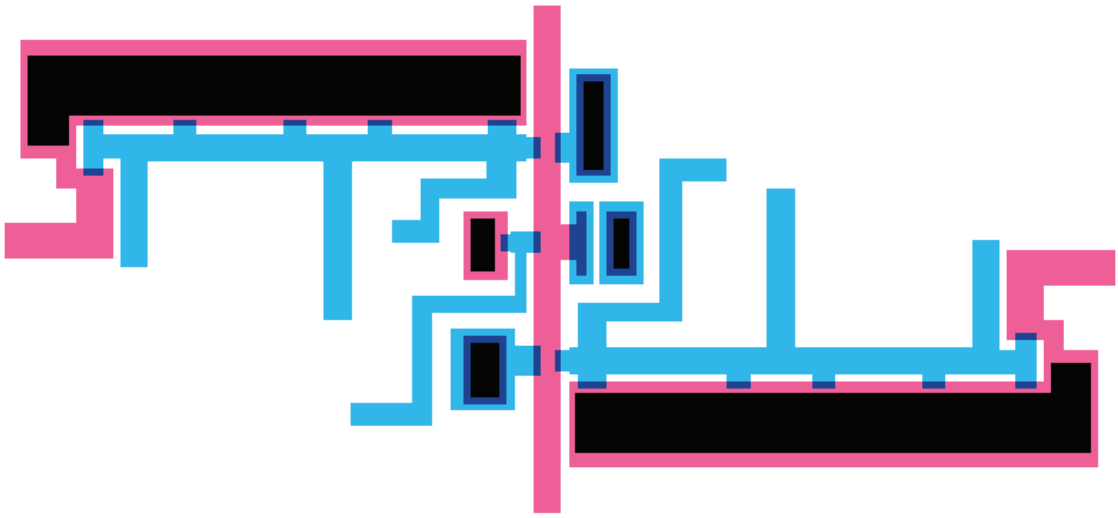
Appendix 2

PULSE STRETCHER

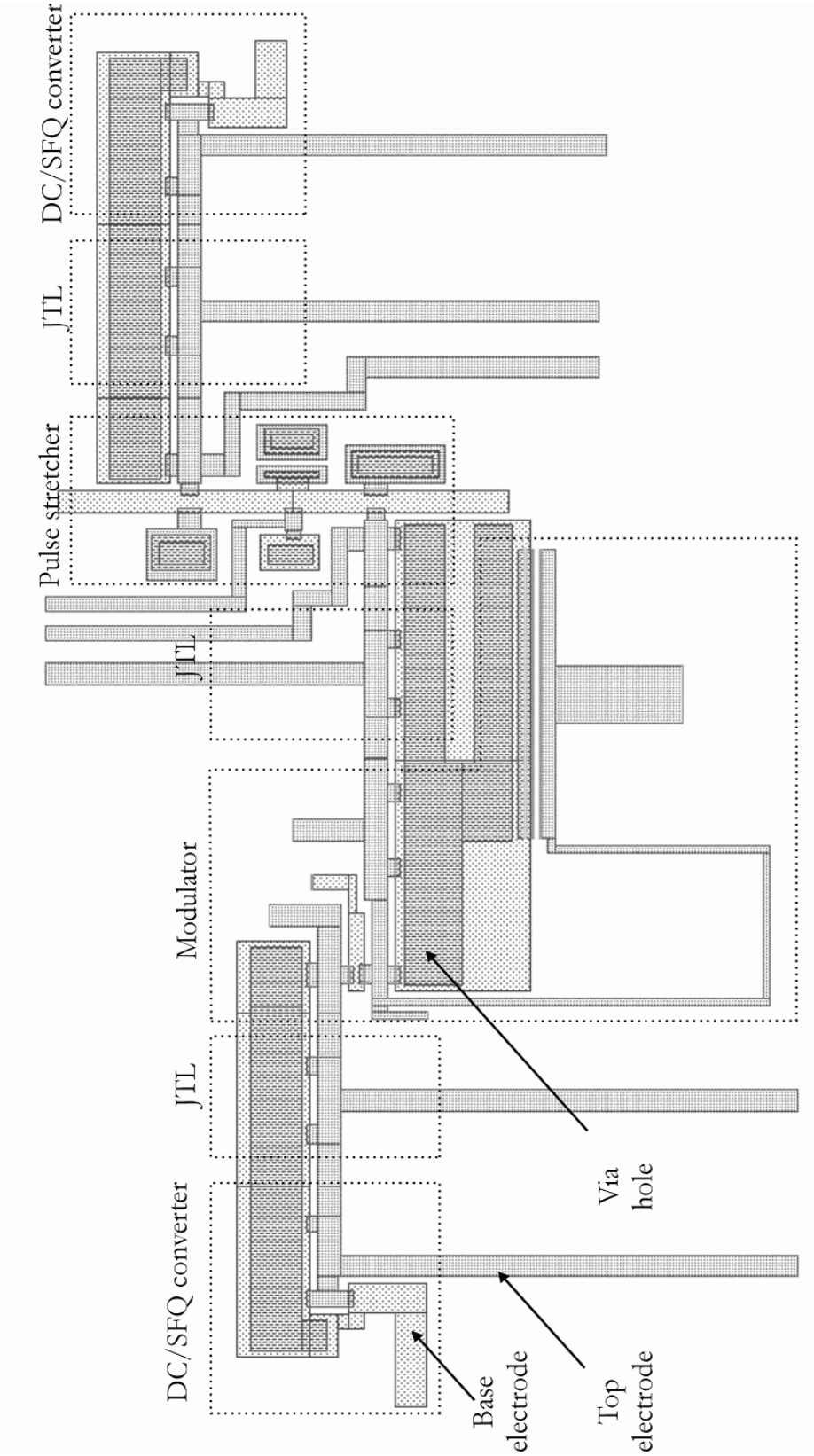
Complete circuit designed for using rotating etching



Circuit Schematics-Pulse stretcher



Mask layout- Pulse stretcher



Mask layout of a first order modulator integrated with a pulse stretcher

Summary

A Josephson junction is the basic element of rapid single flux quantum logic (RSFQ) circuits. A high operating speed and low power consumption are the main advantages of RSFQ logic over semiconductor electronic circuits. To realize complex RSFQ circuits in HTS technology one needs a reproducible fabrication of Josephson junctions with low parameter spread. High quality HTS junctions require a fully epitaxial multilayer structure with clean interfaces and a smooth surface morphology. Neodymium barium copper oxide (NBCO) thin films were used as superconducting electrodes due to their high transition temperature and low surface roughness. NBCO forms a solid solution in which Nd^{3+} ions can substitute for Ba^{2+} ions with the formula $Nd_{1+x}Ba_{2-x}Cu_3O_y$ (x=0.12 in our study). Cation disorder and oxygen deficiency affect the structural and electronic properties of grown NBCO films. Target composition, substrate temperature, oxygen partial-pressure and annealing steps are properly chosen to obtain smooth films with a high transition temperature. NBCO is deposited on an STO buffered MgO substrate at a pressure of 0.35 mbar in an Argon and Oxygen (20:1) gas mixture. The substrate temperature was fixed at 820^0 C. The deposited film is smooth with a surface roughness of 1-3 nm for a 150 nm thick layer and a transition temperature around 90K.

Ramp type junctions with charge transport along the crystallographic ab-plane of the superconducting electrodes are attractive for RSFQ circuits because the current-voltage (I-V) characteristics can be controlled by the barrier material and its thickness. Junctions can be placed freely within the ab-plane to increase the circuit density. An in-situ deposition of a NBCO base electrode and a bi-layer of PBCO/STO have been performed and ramp edges are defined by argon ion milling. The PBCO/STO bi-layer is used as an isolation layer to separate the superconducting electrodes. After the ramp cleaning process and ramp annealing steps, a thin barrier and the top NBCO electrode are deposited. Gallium doped PBCO was used as a barrier material. Then, junction widths are defined and the contact pads are made by using a gold lift-off process. From the measurements, it was found that junctions showed resistively-shunted-junction (RSJ) like I-V characteristics with some amount of excess current. The spread in critical current, ranges between 5 and 20 percent from the mean value over an area of 1 mm^2. The spread in junction parameters is mainly determined by the smoothness of the ramp surface and the growth of the barrier and the top electrode. Degradation of the transition temperature of the NBCO electrode additionally affects the reproducibility and the spread in critical current. Attempts to fabricate junctions using the concept of an additional repairing interlayer have been made. First results showed a large spread with a low $I_C R_N$ product around 260μV at 10K. With the introduction of a ground plane, the inductances of the strip lines are reduced further. Direct injection SQUIDs are fabricated and the inductance of the base and top electrodes are measured.

Oversampling delta-sigma superconducting analog to digital converters can obtain a high dynamic range over a MHz bandwidth by utilizing the high switching speed of Josephson junctions. A first order delta-sigma modulator with a current input consists of an RL integrator and the integrated current input is digitized by the Josephson

comparator. For every SFQ pulse output, the integrator current is reduced by Φ_0 / L. The dynamic range can be further improved by using a higher order modulator. A second order modulator has been designed and its performance has been investigated by simulation using the Josephson simulator (JSIM) and by analyzing the modulator output by a Fast Fourier Transform (FFT). A Second order modulator has two integrators and the feedback to the integrator, connected to the comparator, is given by the quantizer junction itself. The feedback system, providing a feedback gain $(m\Phi_0)$ to the integrator directly connected to current-signal input, increases the complexity of the circuit. Increasing the number of feedback pulses *m* improves the noise shaping property. The effect of the integrator inductor on the performance of the modulator and the chances of realization of the second order modulator in HTS technology have been investigated.

One of the main challenges of RSFQ logic circuits is the transfer of SFQ data to semiconductor circuits due to the low signal level of a Josephson junction and the narrow pulse-width of a few picoseconds. We have studied the use of a pulse stretcher as an interfacing circuit between a RSFQ logic circuit and room temperature electronics. The pulse stretcher provides an extended voltage pulse for every SFQ data pulse. Since the output voltage level is limited by the $I_C R_N$ product of the output junctions, a low noise and low input impedance amplifier is required to detect and improve the signal level further. The pulse width at the pulse stretcher output is limited by the bandwidth of the amplifier. We have studied two kinds of pulse stretcher circuits and estimated the fabrication yield of both pulse stretchers as function of the parameter spread. A pulse stretcher circuit was fabricated in HTS ramp type technology and its digital operation was successfully verified experimentally at 47 K. False switching has occasionally been observed in some samples due to various reasons. Unavoidable parasitic inductances introduced by the design rules for non-rotating etching, spread in the junction parameters, thermal fluctuations and the noise generated by the measurement setup were found to affect the functionality of the fabricated circuit.

Two models have been developed to connect the pulse stretcher with RSFQ circuits whose output data pulses have to be converted into extended voltage pulses for further processing by semiconducting circuits. In both cases, data pulses set the pulse stretcher. The reset pulse is applied using a splitter network in one of the models in which the delay is fixed within the circuit. In the second model, the reset pulse is generated by using an external clock. Impedance mismatch causes reflections at the interface. Simulations have been performed to see the behavior of the extended pulses along a passive transmission line terminated with a load resistor. A semiconducting amplifier with low input impedance close to the normal resistance of the output junction is required for a direct connection of the RSFQ circuit with the semiconductor circuits. In practical cases, parasitic inductances, resistances and capacitances introduce additional mismatch depending on the way of connection.

Samenvatting (Summary in Dutch)

Een Josephson junctie is het basiselement van ‘rapid single flux quantum’ (RSFQ) logische schakelingen. De hoge schakelsnelheid en het lage energieverbruik van RSFQ logica zijn de belangrijkste voordelen ten opzichte van halfgeleidende elektronische schakelingen. Om gecompliceerde RSFQ schakelingen in hoge-temperatuur supergeleidende (HTS) technologie te realiseren, is het noodzakelijk om op reproduceerbare wijze Josephson juncties met weinig onderlinge variatie in de eigenschappen te maken. Een volledige epitaxiale multilaagsstructuur met schone grensvlakken en een gladde oppervlaktemorfologie is vereist voor HTS juncties van hoge kwaliteit. Dunne lagen van neodyniumbariumkoperoxide (NBCO) zijn gebruikt als supergeleidende elektrodes vanwege de hoge transitietemperatuur en lage oppervlakte-ruwheid. NBCO is een ‘vastestofoplossing’ met de formule $Nd_{1+x}Ba_{2-x}Cu_3O_y$ (waarbij x = 0.12 in deze studie), waarin de Ba^{2+} ionen door Nd^{3+} ionen kunnen worden gesubstitueerd. Wanorde van de kationen en het gebrek aan zuurstof beïnvloeden de structurele en elektronische eigenschappen van gegroeide NBCO dunne lagen. De samenstelling van het ‘target’, de substraattemperatuur, de partiële zuurstofdruk en ‘anneal’-stappen zijn zodanig gekozen dat gladde films met een hoge transitietemperatuur worden verkregen. NBCO is hierbij in een gasmengsel van argon en zuurstof (20:1) bij een druk van 0.35 mbar gedeponeerd op een MgO substraat met een STO bufferlaag en een substraattemperatuur van 820 ºC. Gedeponeerde lagen met diktes van 150 nm zijn glad en hebben een oppervlakteruwheid van 1-3 nm en een transitietemperatuur van circa 90 K.

‘Ramptype’ juncties, waarin het ladingstransport plaatsvindt in het kristallografische *ab*-vlak van de supergeleidende elektrodes, zijn aantrekkelijk voor gebruik in RSFQ schakelingen omdat de stroom-spanningskarakteristieken door het barrièremateriaal en de -dikte worden bepaald. Juncties kunnen verder vrij in het *ab*-vlak worden geplaatst waardoor de elementdichtheid van de schakeling wordt vergroot. De NBCO basiselektrode en een PBCO-STO dubbellaag zijn *in-situ* gedeponeerd, waarna de ramp structuren zijn gedefinieerd door te etsen met argon ionen. De PBCO-STO dubbellaag wordt gebruikt als isolatielaag tussen de supergeleidende elektrodes. Na het schoonmaken en herstellen van de ramp, zijn de dunne barrièrelaag en de tegenelektrode gedeponeerd. Gallium gedoteerd PBCO is hierbij als barrièremateriaal gebruikt. Daarna zijn de junctiebreedtes gedefinieerd en de contactpaden gemaakt door middel van goud ‘lift-off’. De gemeten stroom-spanningskarakteristieken vertonen gedrag zoals ook volgt uit het resistief-geshunte-junctie (RSJ) model met daarbij nog een additionele stroom-component. De variatie in de kritieke stroom is 5 tot 20 % van het gemiddelde over een oppervlak van 1 mm^2. De variatie in junctieparameters wordt vooral bepaald door de gladheid van het ramp-oppervlak en de groei van de barrière en tegenelektrode. Ook de degradatie van de kritieke temperatuur van de NBCO basiselektrode beïnvloedt de reproduceerbaarheid en de variatie in de kritieke stroom. Pogingen om juncties te fabriceren volgens het concept van een additionele reparerende tussenlaag leverden in eerste instantie een hoge spreiding op en een laag I_CR_N-produkt van circa 260 μV bij 10 K. Door het invoeren van een grondvlak is het mogelijk gebleken de inductie van de

eletrodebanen te reduceren. SQUIDs met directe injectie zijn gefabriceerd waarmee de inductie van basis- en tegenelektrode zijn gemeten.

Overgesamplede delta-sigma supergeleidende analoog-naar-digitaal omzetters met grote dynamische werkgebieden bij een bandbreedte van 1 MHz kunnen worden verkregen door gebruik te maken van de hoge schakelsnelheid van Josephson juncties. Een eerste-orde delta-sigma modulator met een stroominvoer bevat een RL integrator, waarbij de geïntegreerde stroominvoer wordt gedigitaliseerd door een Josephson comparator. Bij elke SFQ uitgangspuls wordt de integratorstroom gereduceerd met Φ_0/L. Het dynamische werkgebied kan verder worden verbeterd door een modulator van een hogere orde te gebruiken. Een tweede-orde modulator is ontworpen, de prestaties zijn gesimuleerd in een Josephson simulator (JSIM) en de modulatoruitvoer is geanalyseerd door middel van een 'fast Fourier' transformatie (FFT). Een tweede-orde modulator heeft twee integratoren. De terugkoppeling naar de integrator, verbonden met de comparator, wordt gegeven door de junctie die het signaal kwantiseert. De terugkoppeling met een versterking van $m\Phi_0$ naar de (aan de stroominvoer gekoppelde) integrator vergroot de complexiteit van de schakeling. Verhoging van het aantal (m) terugkoppelpulsen verbetert echter wel de ruisvorm. De invloed van de inductie van de integrator op de prestaties van de modulator en op de kans dat de tweede-orde modulator gerealiseerd kan worden in HTS technologie is onderzocht.

Vanwege het lage signaalniveau van een Josephson junctie en de smalle pulsbreedte van enkele picoseconden is de doorvoer van SFQ data naar halfgeleiderschakelingen één van de belangrijkste uitdagingen in het gebruik van RSFQ logische schakelingen. In dit proefschrift is de toepassing van een 'pulsstrekker' als overbrugging tussen een RSFQ schakeling en kamertemperatuurelektronica onderzocht. De pulsstrekker levert een verlengde spanningspuls bij elke SFQ datapuls. Een versterker met een lage impedantie en weinig ruis is nodig om het uitgangssignaal te detecteren en verder te versterken omdat de uitgangsspanning wordt gelimiteerd door het $I_C R_N$-produkt van de uitvoerjuncties. De pulsbreedte van de verlengde puls wordt gelimiteerd door de bandbreedte van de versterker. Twee pulsstrekkerschakelingen zijn bestudeerd en de verwachte fabricageopbrengst van beide schakelingen is afgeschat als functie van de spreiding van de parameters. Eén van de pulsstrekkers is gefabriceerd door middel van HTS technologie. Bij 47 K is experimenteel vastgesteld dat de schakeling digitaal correct functioneert. Om verschillende redenen trad in enkele schakelingen incidenteel ongewenst schakelgedrag op. De functionaliteit van de gefabriceerde schakeling bleek vooral te worden beïnvloed door variatie in de junctieparameters, thermische fluctuaties, ruis die door de meetopstelling zelf wordt gegenereerd en parasitaire inducties die onvermijdbaar zijn in een ontwerp dat geschikt is voor niet-rotationeel etsen.

Twee modellen zijn ontwikkeld om de pulsstrekker te verbinden met de RSFQ circuits waarvan de uitvoerpulsen omgezet dienen te worden in verlengde pulsen om verder verwerkt te kunnen worden door halfgeleiderschakelingen. In beide modellen wordt de pulsstrekker door datapulsen ingesteld. De reset puls wordt in het ene model geleverd via een splitsingsnetwerk, waarin de vertraging vantevoren is vastgelegd. In het andere model wordt de reset puls gegenereerd door een externe klok.

Impedantieverschillen tussen de schakelingen veroorzaken reflecties aan het grensvlak. Simulaties zijn uitgevoerd om te onderzoeken hoe de verlengde pulsen zich langs een passieve transmissielijn die uitmondt in een weerstand gedragen. Een halfgeleiderversterker met een lage invoerimpedantie die dicht bij de normale weerstand van de uitvoerjunctie ligt, is vereist om de RSFQ schakeling te kunnen verbinden met halfgeleiderelektronica. In de praktijk zullen, afhankelijk van de manier van verbinden, parasitaire inducties, weerstanden en capaciteiten extra impedantieverschillen introduceren.

Acknowledgements

I would like to express my gratitude to late Gerrit Gerritsma for offering me a PhD position in the field of superconducting electronics. I remember the great hospitality I received when I came to Twente for the first time. Unfortunately, I have missed the chance of working with him.

I wish to acknowledge with my deepest gratitude the continued support, encouragement, suggestions and advice given by my supervisor Horst Rogalla during the entire period of my PhD work. I would like to thank Alexander Brinkman for his helpful suggestions and fruitful discussions on the sample preparation. I also thank him for checking every page of my thesis to give it shape and translating the summary into Dutch.

Thanks goes to Ingrid for helping me to work with the sputter system, for teaching me photolithography and for her support during the sample preparation. I wish to thank Eko for his help with the thin film work. I would like to thank Thomas for introducing me to the optimization program and for the valuable discussions about the circuit design and simulations.

I would like to thank Guus Rijnders for his support and discussions in the beginning of the project. Thanks goes to Jaap Flokstra and the THz group for a lot of discussions during THz meetings. Special thanks goes to Dick Veldhuis and Frank Roesthuis for their help and technical support in the lab. I would like to thank Sybolt Harkema and Gerrit van Hummel for their help with x-ray measurements.

Thanks to Ans and Inke for all their help, especially in extending housing contracts and the residence permit. I extend my gratitude to all my colleagues who have made my studies a pleasant and memorable experience. I especially thank Ariando for occasional discussions and for his help when shifting rooms, and of course Agnes, Mark, Joska, Johannes, Kees, Aico, Maarten, Martin and Kelvin.

Financial support to this work was provided by the European community through the SuperADC project.

Finally, I wish to thank family members and friends for their support and motivation in many ways.